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Compal LA-K281P

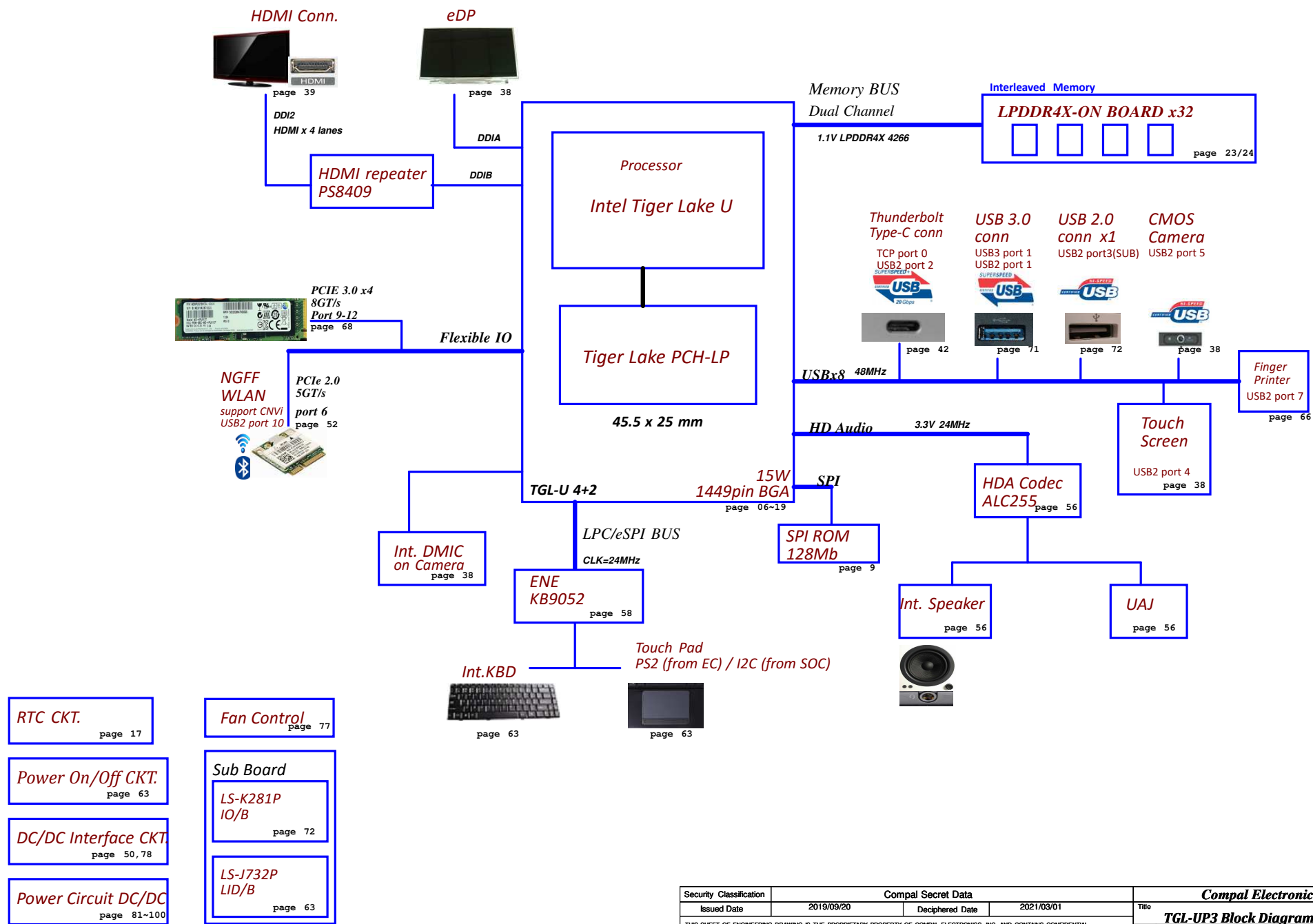
GH4FT MB Schematic Document

Rev: 1A

2020.08.03

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Model Name: TGL-UP3
Project Name: LA-K281P



Board ID Table for AD channel

Vcc	3.3V							
Ra	100K +/- 1%							
Board ID /PCB Revision	Rb	V _{BID} min	V _{BID} TYP	V _{BID} Max	EC AD3			
0 → 0.1	0		0 V	0.300 V	0x00 - 0x13			
1 → 0.2	12K +/- 1%	0.347 V	0.354 V	0.36 V	0x14 - 0x1E			
2 → 0.3	15K +/- 1%	0.423 V	0.430 V	0.438 V	0x1F - 0x25			
3 → 0.4	20K +/- 1%	0.541 V	0.550 V	0.559 V	0x26 - 0x30			
4 → 0.5	27K +/- 1%	0.691 V	0.702 V	0.713 V	0x31 - 0x3A			
5 → 0.6	33K +/- 1%	0.807 V	0.819 V	0.831 V	0x3B - 0x45			
6 → 0.7	43K +/- 1%	0.978 V	0.992 V	1.006 V	0x46 - 0x54			
7 → 0.8	56K +/- 1%	1.169 V	1.185 V	1.200 V	0x55 - 0x64			

Will be Update

SOC SMBUS Address Table (TBC)

SOC_SMBUS Net Name	Power Rail	Device	Address (7 bit)	Address (8bit)	
				Write	Read
SOC_SML0CLK SOC_SML0DATA	+3V_PRIM	PD	0x08	TBC	0x08
		Re-Timer	0x55	TBC	0x30
SOC_SML1CLK SOC_SML1DATA	+3V_PRIM	EC	TBC	TBC	TBC
		Thermal	TBC	TBC	TBC

BOM Structure Table

Func t i on	Stuff	Un-Stuff
dGPU SKU	DIS@	
dGPU support GC6	GC6@	
CMC	CMC@	
HDD FFC CON (With Redriver)	HDD_RD@	HDD_FFC@
HDD FFC CON (Non Redriver)	HDD_FFC@	HDD_RD@
EMI / EMC / ESD Components	EMI@	@EMI@
	BL_EMI@	
	EMC@	@EMC@
	BL_EMC@	
RF Components	ESD@	@ESD@
	BL_ESD@	
	RF@	@RF@
PRIM Design	PREM@	VOL@
Volume Design	VOL@	PREM@
CNVI	CNVI@	
WWAN		
SSD	WWAN@	
	SSD@	
Type C	TypeC@	
Type A	TypeA@	
Finger Print	FP@	
GLITCH	GLITCH@	
KB Backlight	KB_BKL@	
SPI Touch	SOC_THP@	
MIPI Camera	CVF@	
FIP	FIP@	
ES1 SOC	ES1@	
For Signal Test	MP@	
NC Components	@	
ME Connector	CONN@	
JUMP (HW & PWR)	JUMP@	@JUMP@
JUMP (PWR)	VGAJUMP@	

Load BOM Option Table

BOM Number	Load BOM Option
431ANQBOL04	i7QU71@/PCB@/X76MIC16G@/Z55@/3S@/CHG@/CMC@/CNVI@/EVT@/FP@/GLITCH@/MP@/TMS@/TPM@/TypeC@/VOL@/X4E@/

Load BOM Option Table for Baseline

BOM Number	Load BOM Option
431ACX30L01(DISCRETE)	DIS@/EMI@/ESD@/EMC@/GC6@/GLITCH@/HDD_FFC@/VOL@/ES1@
431ACX30L02(UMA)	EMI@/ESD@/EMC@/GLITCH@/HDD_FFC@/VOL@/ES1@

HSIO Port Table (CPU)

HSIO Port	Capable	Port Allocat i on	PCIE CLK	NOTE
0	PCle4 #1			
1	PCle4 #2	No use	NA	PCle interface
2	PCle4 #3			
3	PCle4 #4			

HSIO Port Table (PCH)

HSIO Port	Capable	Port Allocat i on	PCIE CLK	NOTE
0	USB3.1 #1 / PCle #1	USB3.1 Type A	NA	USB3.1 interface
1	USB3.1 #2 / PCle #2	NA	NA	NA
2	USB3.1 #3 / PCle #3	NA	NA	NA
3	USB3.1 #4 / PCle #4	NA	NA	NA
4	PCle #5	NA	NA	NA
5	PCle #6	WLAN	CLK3 & CLKREQ#3	PCle interface
6	PCle #7 /GbE	NA	NA	NA
7	PCle #8 /GbE	NA	NA	NA
8	PCle #9 /GbE			
9	PCle #10	SSD (NGFF Key M)	CLK1 & CLKREQ#1	PCle interface
10	PCle #11 /SATA0			
11	PCle #12 /SATA1			

Power State

STATE	SIGNAL	SLP_S0#	CPU_C10_GATE#	SLP_S3#	SLP_S4#	SLP_S5#	+VALW	+V	+VS	Clock
S0 (Full ON)		HIGH	HIGH	HIGH	HIGH	HIGH	ON	ON	ON	ON
S3 (Suspend to RAM)		HIGH	HIGH	LOW	HIGH	HIGH	ON	ON	OFF	OFF
S4 (Suspend to Disk)		HIGH	HIGH	LOW	LOW	HIGH	ON	OFF	OFF	OFF
S5 (Sof t Off)		HIGH	HIGH	LOW	LOW	LOW	ON	OFF	OFF	OFF
S0IX		LOW	LOW	HIGH	HIGH	HIGH	ON	ON	ON	ON

USB2.0 Port Table

USB2.0 Port	Device
1	USB Type-A (MB)
2	TBT Type-C (MB)
3	USB Type-A (IO Board)
4	TS
5	Camera
6	N/A
7	FP
8	N/A
9	N/A
10	BT

I2C Address Table (TBC)

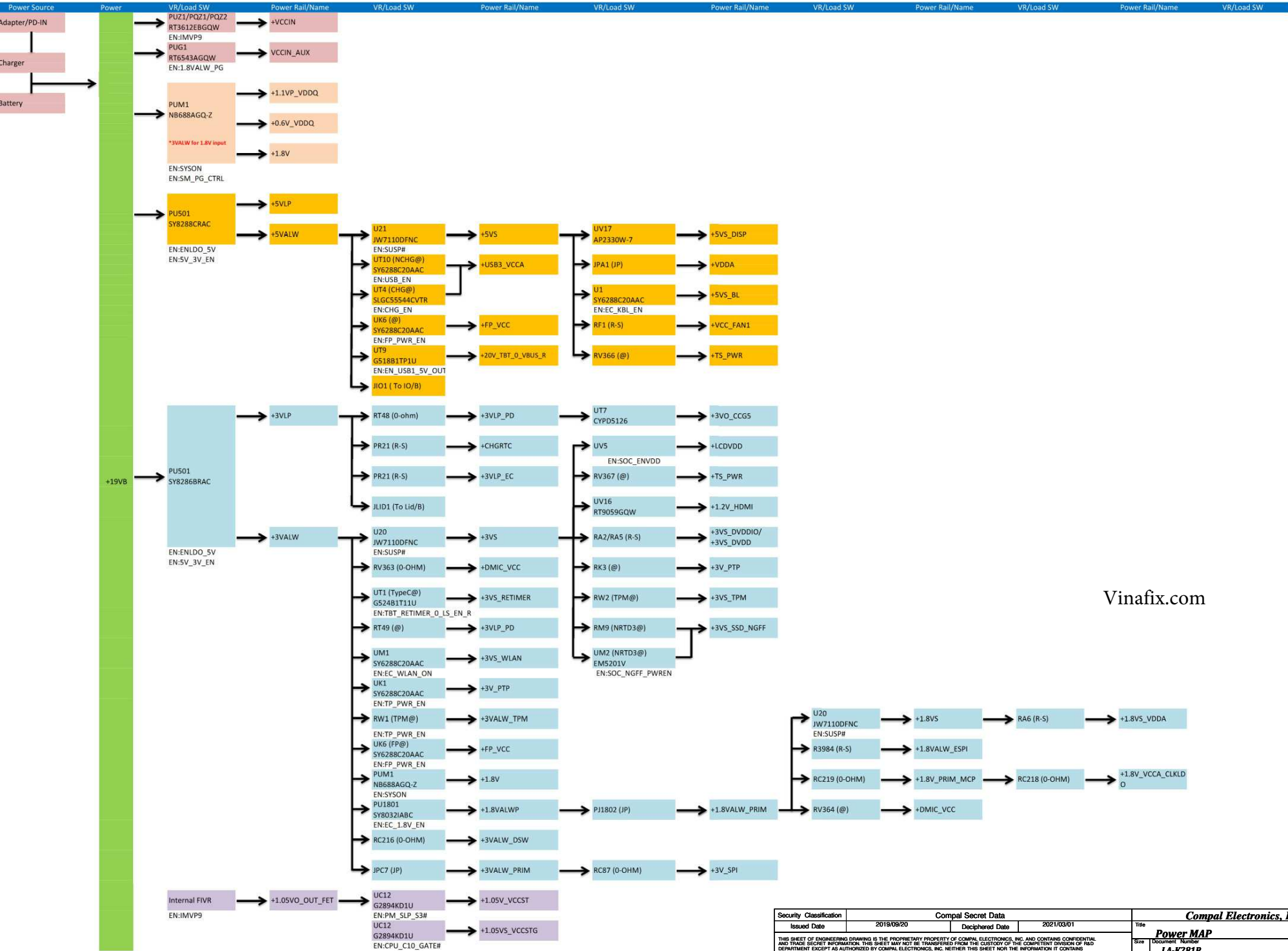
I2C Port	Power Rail	Device	Address (7 bit)	Address (8bit)	
				Write	Read
I2C 0	+3VS	EC HID device	TBC	TBC	TBC
I2C 1	NC	NA	TBC	TBC	TBC
I2C 2	NC	NA	TBC	TBC	TBC
I2C 3	+3VALW	Touch Pad	0x2CH	TBC	TBC
I2C 4	NC	NA	TBC	TBC	TBC
I2C 5	NC	NA	TBC	TBC	TBC
ISH_I2C 0	NC	NA	TBC	TBC	TBC
ISH_I2C 1	NC	NA	TBC	TBC	TBC

Voltage Rails

Power Plane	Descript i on	S0	S0ix	S3	S4/S5
+19V_ADPIN_P1	Adapter power supply	N/A	N/A	N/A	N/A
+20V_PDVIN	PD USB-C power supply	N/A	N/A	N/A	N/A
+12.6V_BATT	Bat tery power supply	N/A	N/A	N/A	N/A
+19VB	AC or bat tery power rail for power circuit	N/A	N/A	N/A	N/A
+VCCIN	Core voltage for CPU	ON	OFF	OFF	OFF
+VCCIN_AUX	CPU and PCH merged auxiliary power rail	ON	OFF	OFF	OFF
+0.6V_VDDQ	LPDDR4x +0.6V power rail(VDDQ)	ON	OFF	OFF	OFF
+1.05V_VCCSTG	Sustain voltage for CPU standby modes	ON	ON	ON	OFF
+1.05VS_VCCSTG	Gated sustain voltage for CPU standby modes	ON	OFF	OFF	OFF
+1.2V_VCCPLL_OC	+1.2V power rail for CPU digital PLL	ON	OFF	ON	OFF
+1.35VS_VRAM	+1.35VS power rail for GPU	ON	OFF	OFF	OFF
+1.1V_VDDQ	LPDDR4x +1.1V power rail (VDD2)	ON	ON	ON	OFF
+1.8V	LPDDR4x +1.8V power rail(VDD1)	ON	ON	ON	OFF
+1.8V_PRIM_SOC	TCSS/AGSH TypeC sub system / CPU analog power supply	ON	OFF	OFF	OFF
+1.8VALW	System +1.8V power rail	ON	ON	ON	ON*
+1.8VS	System +1.8VS power rail	ON	ON	ON	OFF
+3VALW	System +3VALW always on power rail	ON	ON	ON	ON*
+3VLP	+19VB to +3VLP power rail for suspend power	ON	ON	ON	ON
+3VALW_DSW	+3VALW power for PCH DSW rails	ON	ON	ON	ON*
+3V_PRIM	+3VALW power for PCH suspend rails	ON	ON	ON	ON*
+3VS	System +3VS power rail	ON	ON	OFF	OFF
+1.8VS_DGPU_AON	+1.8VS power rail for GPU(AON rails)	ON	OFF	OFF	OFF
+1.8VS_DGPU	+1.8VS power rail for GPU	ON	OFF	OFF	OFF
+VGA_CORE	Power rail for GPU	ON	OFF	OFF	OFF
+5VALW	System +5VALW power rail	ON	ON	ON	ON*
+5VS	System +5VS power rail	ON	ON	OFF	OFF
+3VL_RTC	RTC power	ON	ON	ON	ON

Note : ON* means that this power plane is ON only with AC power available, otherwise it is OFF

[GH4FT-Power Map_TGL-UP3_LPDDR4_Premium_S0ix]



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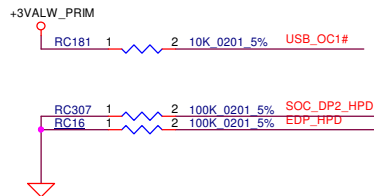
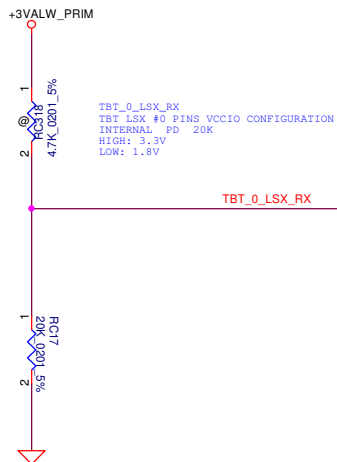
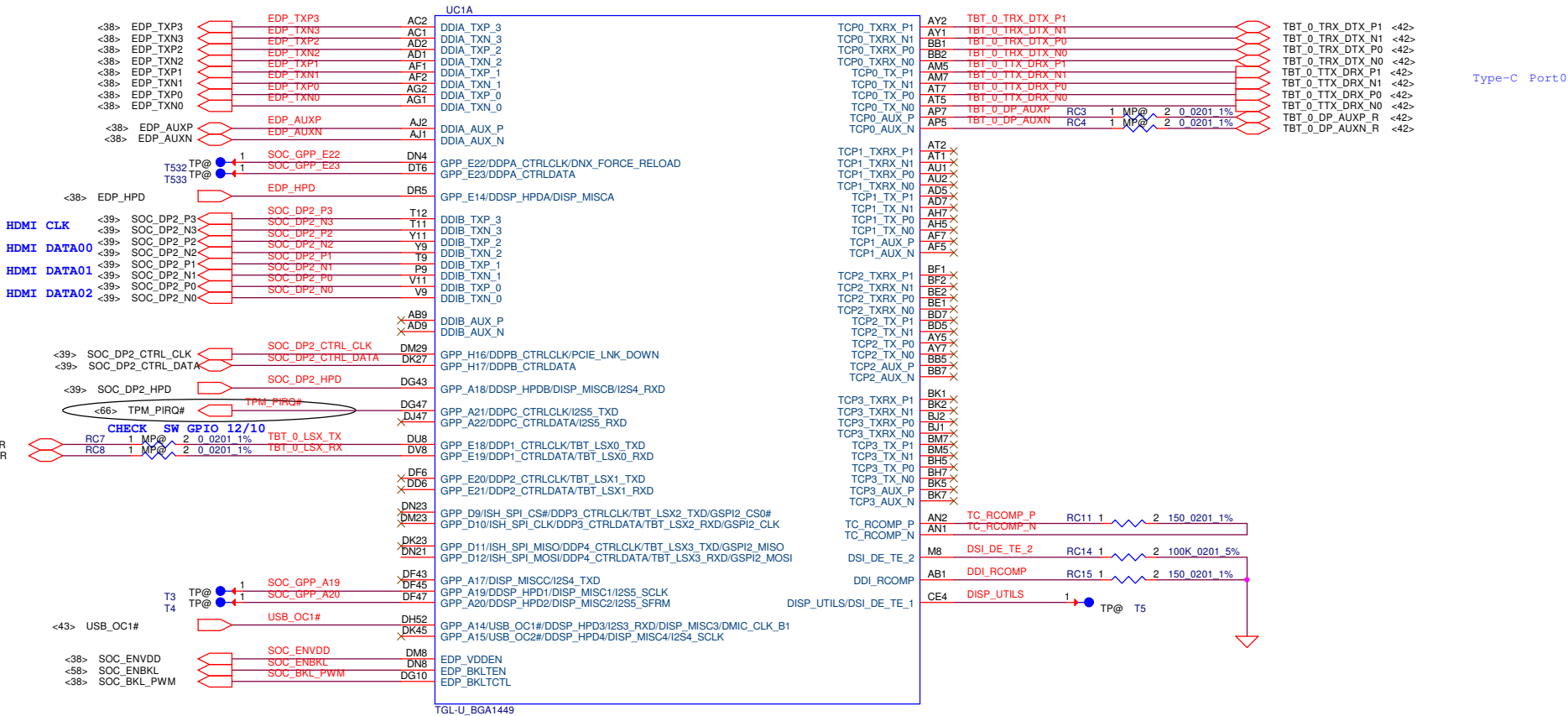
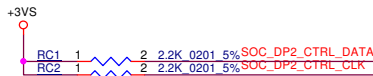
G3->S0

S0-> S0iX

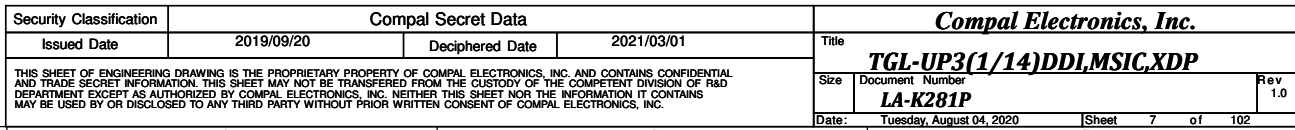
S0iX ->S0

S0->S5



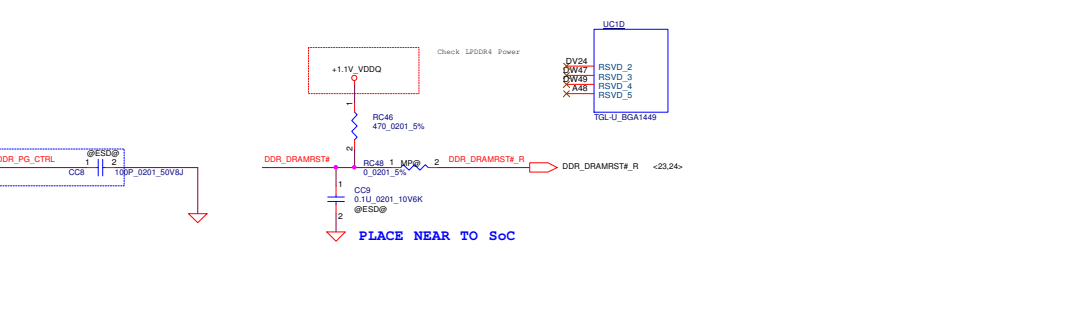
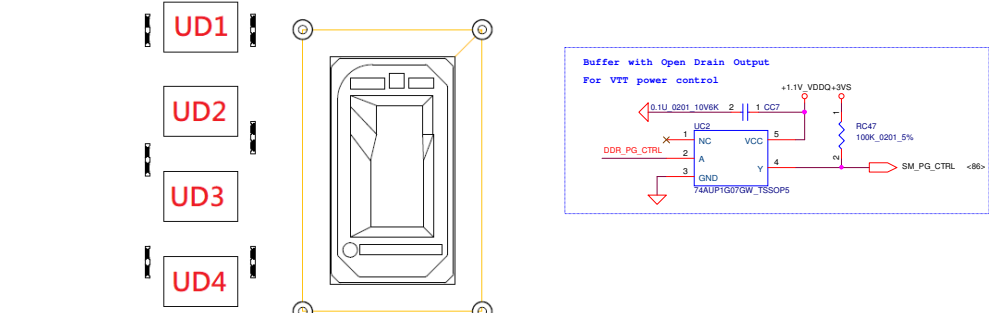
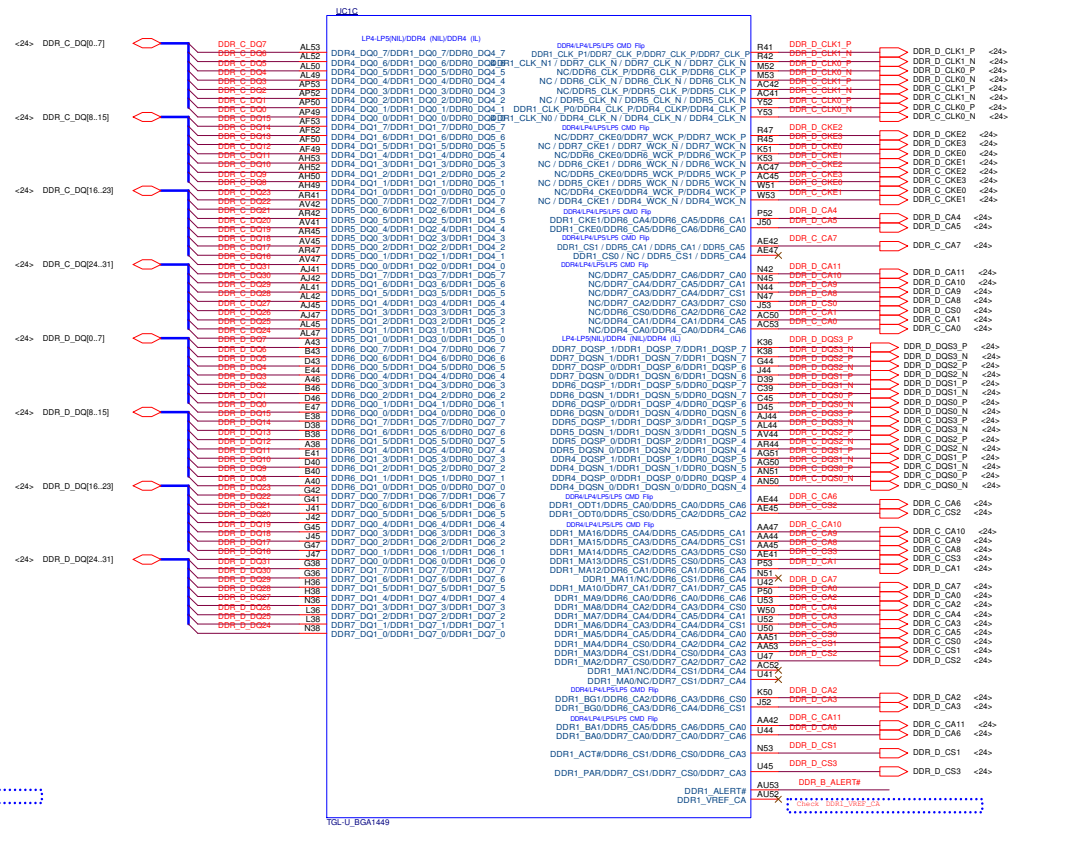
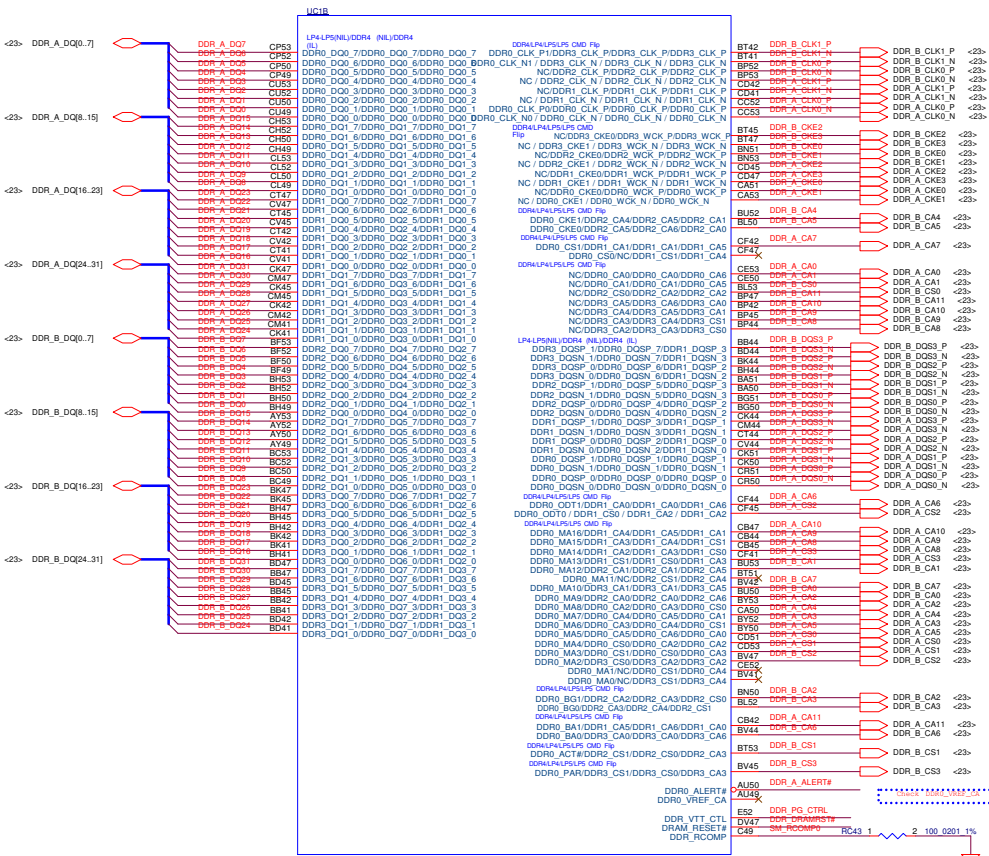


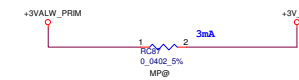
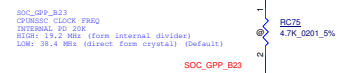
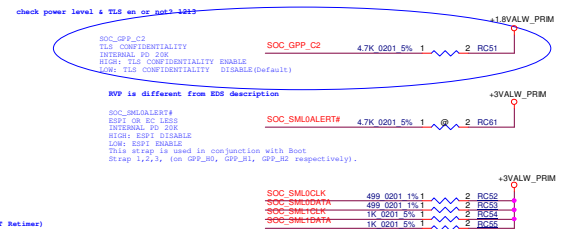
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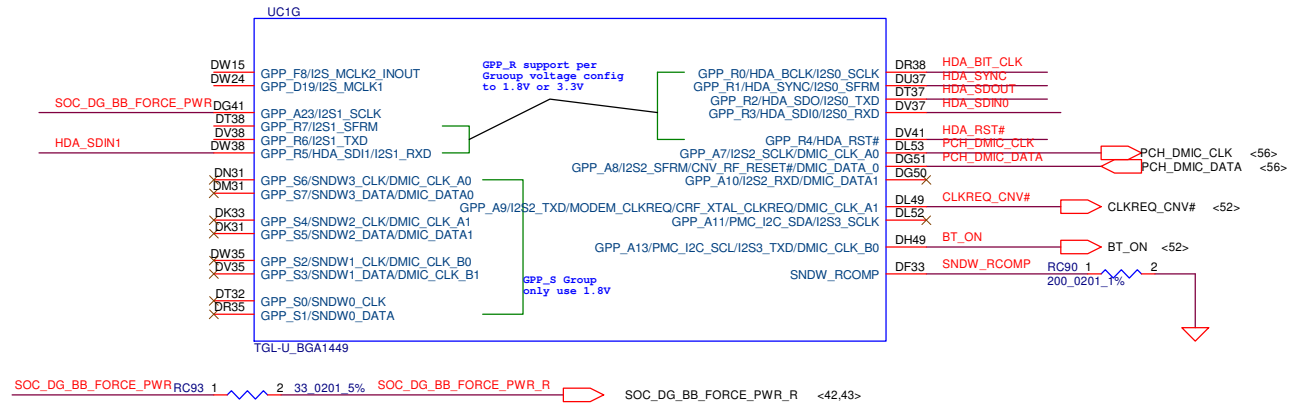
Follow Intel LPDDR4 NIL

LPDDR4: Refer to 612304_TGL_LPDDR4_RVP_SCH_REV0P7

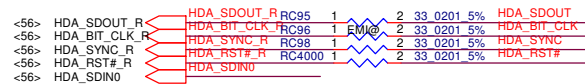




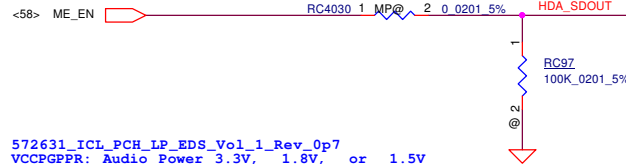
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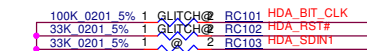
HDA for AUDIO



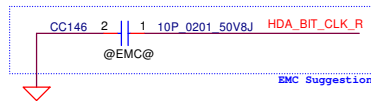
To Enable ME Override



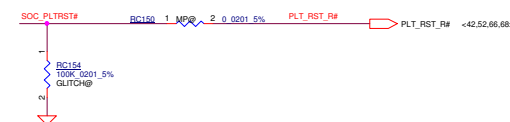
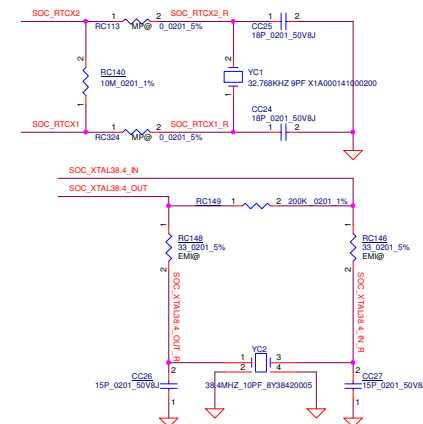
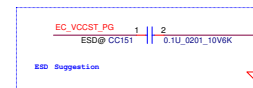
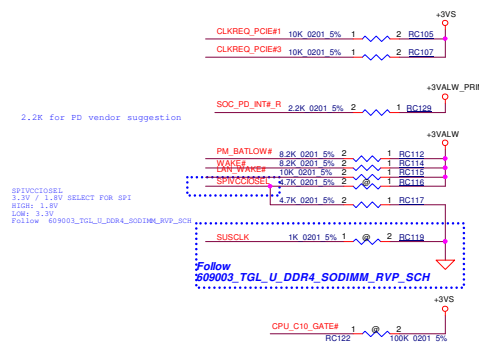
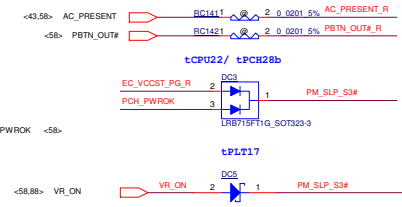
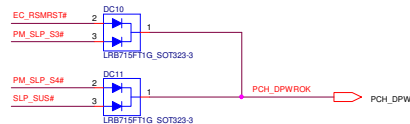
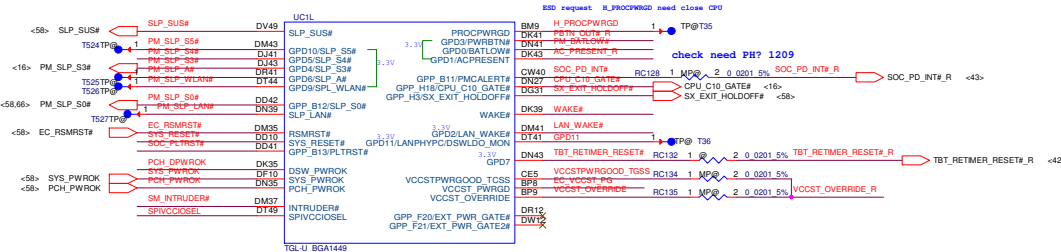
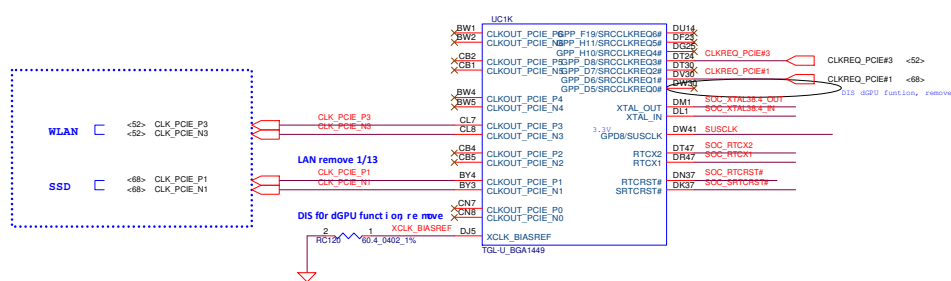
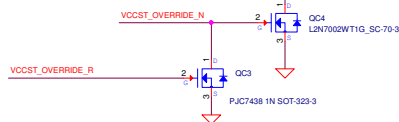
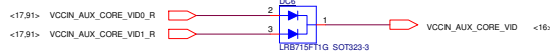
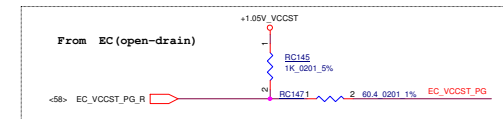
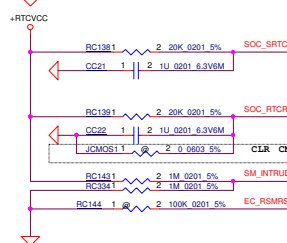
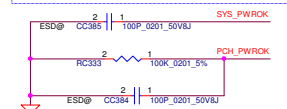
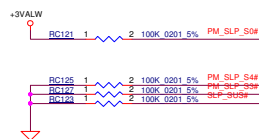
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VCCPGFPR: Audio Power 3.3V, 1.8V, or 1.5V
Need to sync with codec VDDIO



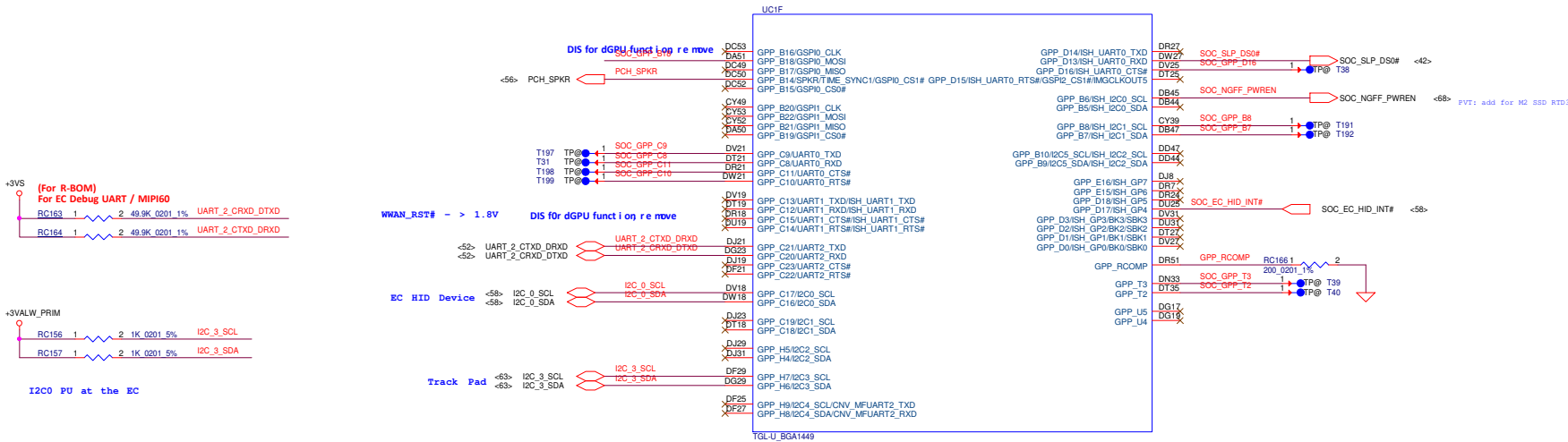
Follow
607872_TGL_UY_PDG for Glitch



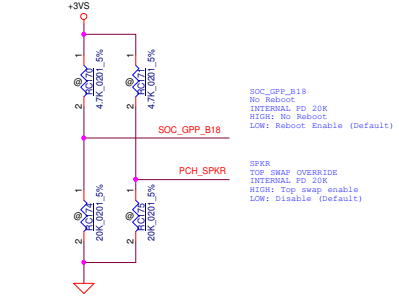
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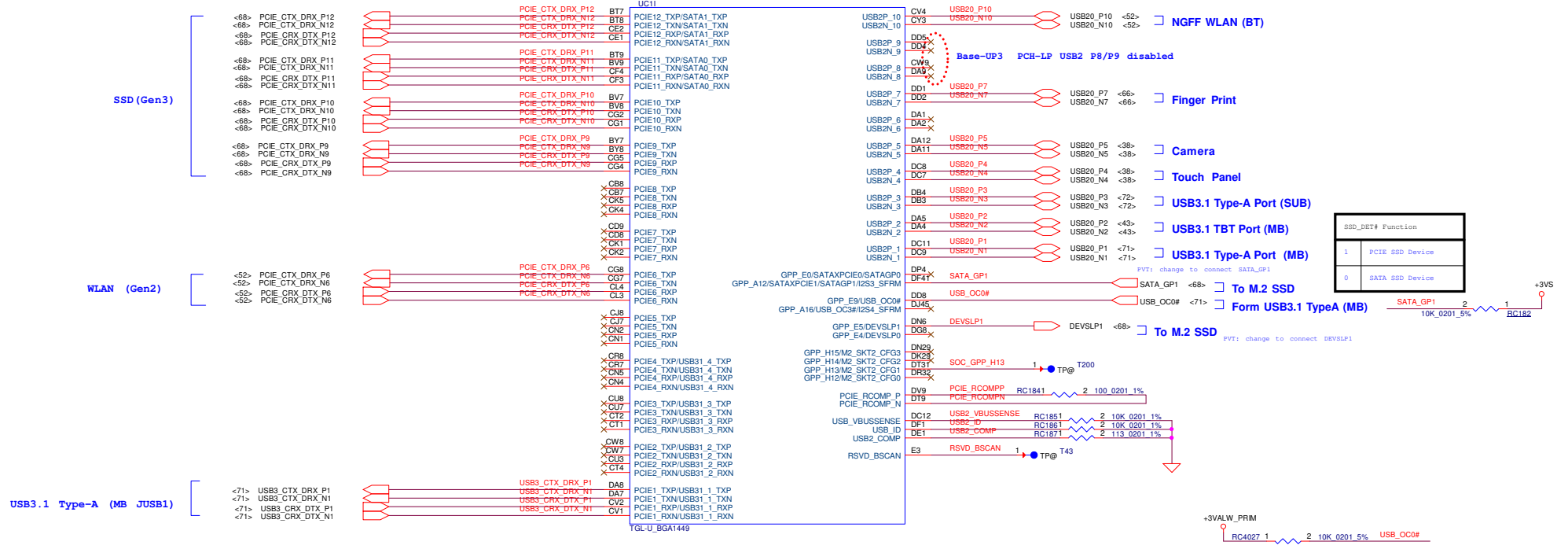
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Strap Pin



PDG 6.8.6
For Integrated Bluetooth* functionality with the Intel® Wireless-AC (CNVI) solution,
Tiger Lake PCH-LP USB 2.0 port # 10 must be used.



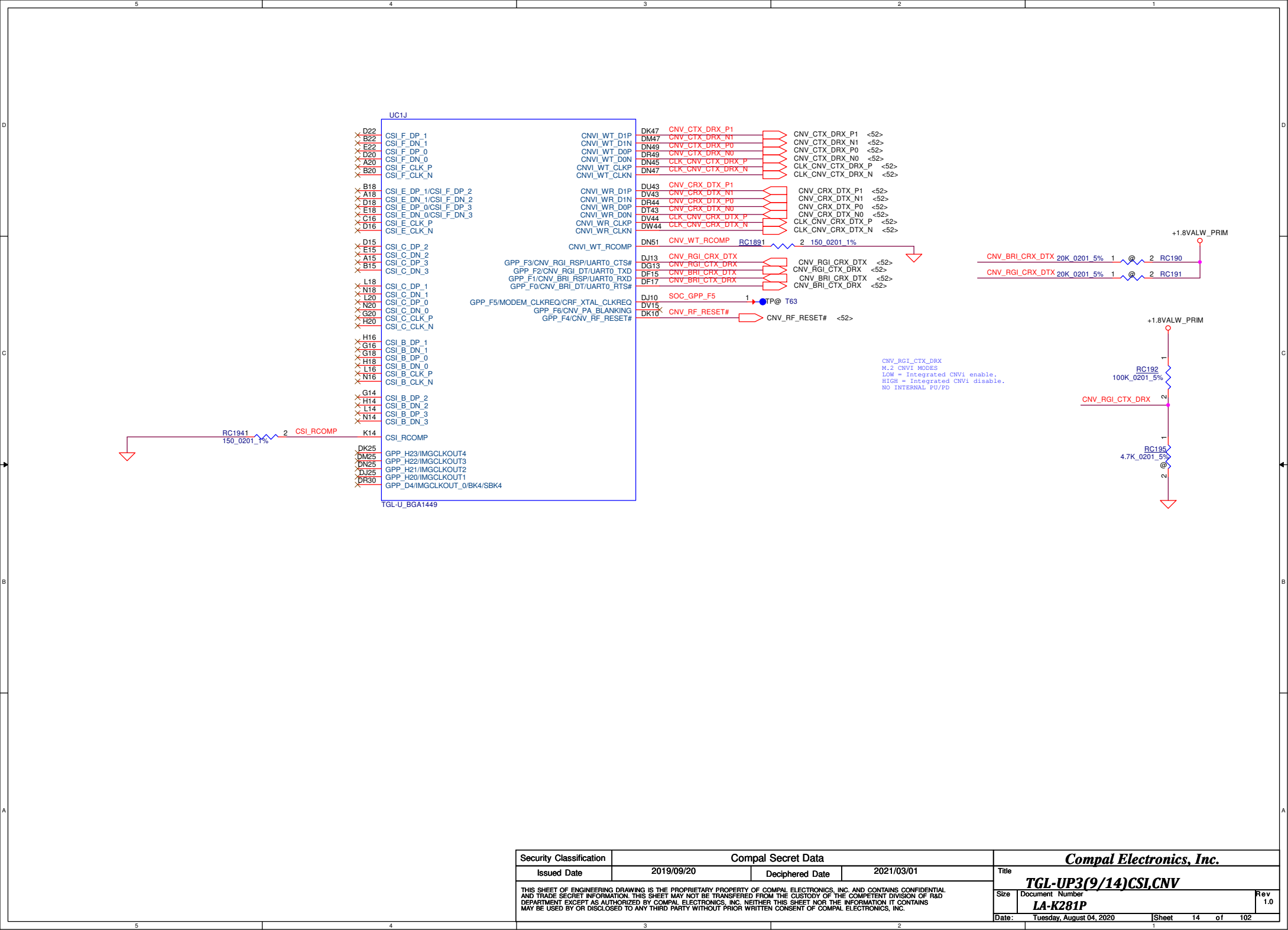
6.4.1 Flexible I/O Implementation
PCH-LP (UP3)

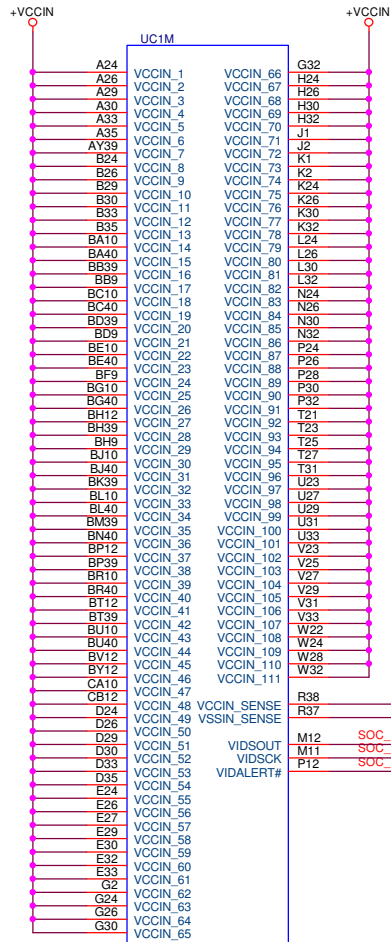
Figure 70. High Speed I/O (HSIO) Lane Multiplexing in PCH-LP (UP3)

Flex HSIO Lane	0	1	2	3	4	5	6	7	8	9	10	11
	USB 3.2 Gen 1x1/Zx1 #1	USB 3.2 Gen 1x1/Zx1 #2	USB 3.2 Gen 1x1/Zx1 #3	USB 3.2 Gen 1x1/Zx1 #4	PCIe* #5	PCIe* #6	PCIe* #7	PCIe* #8	PCIe* #9	PCIe* #10	PCIe* #11	PCIe* #12
HSIO Type and Lane	PCIe* #1	PCIe* #2	PCIe* #3	PCIe* #4								

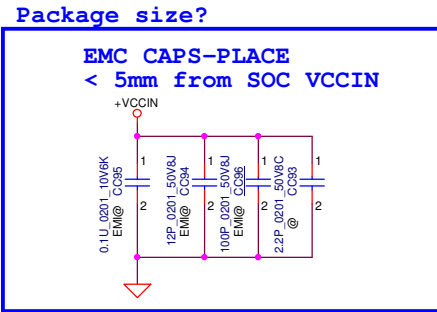
Table 58. Signal Descriptions

Name	Type	SSC Capable	Description
PCH-LP (U): <ul style="list-style-type: none">CLKOUT_PCIE_P[6:0]CLKOUT_PCIE_N[6:0] PCH-LP (Y): <ul style="list-style-type: none">CLKOUT_PCIE_P[6:1]CLKOUT_PCIE_N[6:1]	O	Yes	PCI Express* Clock Output: Serial Reference 100 MHz PCIe* specification compliant differential output clocks to PCIe* devices <ul style="list-style-type: none">CLKOUT_PCIE_P/N [6:0] = Can be used for PCIe* Gen1/2/3 supportCLKOUT_PCIE_P/N [4, 3, 0] = Must be used for PCIe* Gen4 support

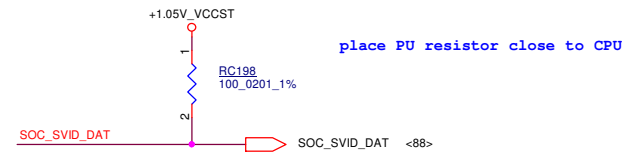




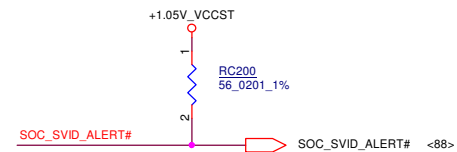
TGL-U_BGA1449



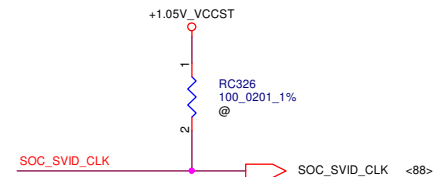
SVID DATA



SVID ALERT

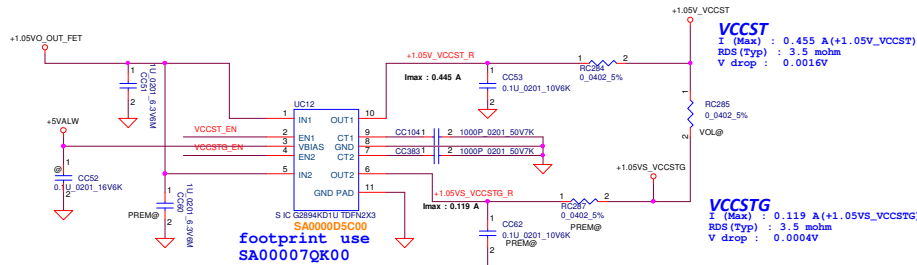
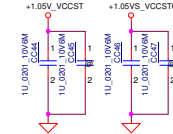
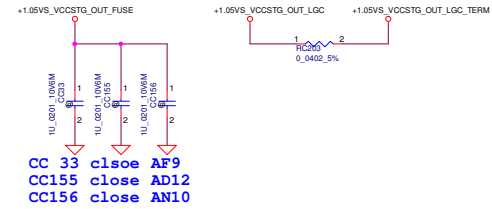
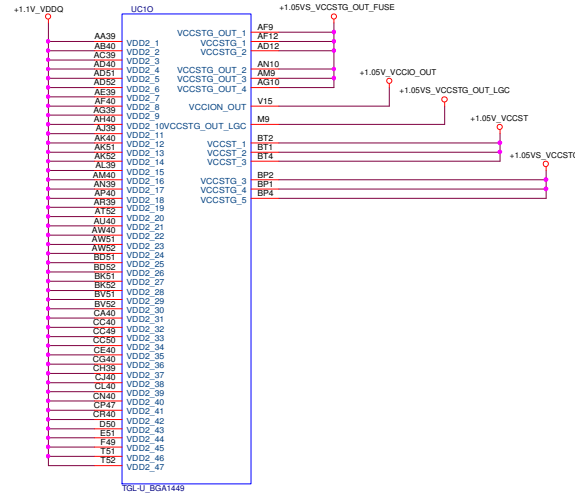
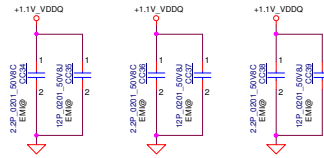


SVID CLOCK



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EMC CAPS-PLACE
< 4mm from SOC VDDQ
with each pair < 12mm Apart
12pF* 3 (EMI@)
2.2pF* 3 (EMI@)



CPU_C10_GATE# stable to +1.05VS_VCCSTG <= 65us (ICPU26)

Place on CPU Side
1uF* 10
10uF* 16
47uF * 2

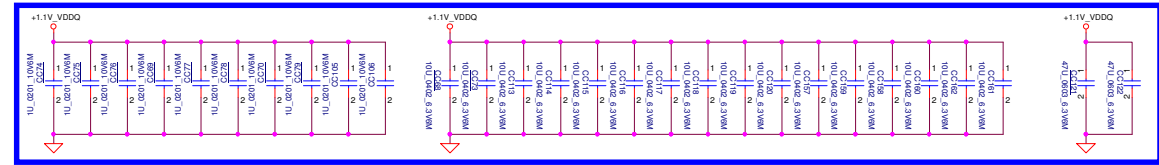
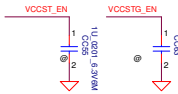


Figure 228. VCCSTG Enable Logic

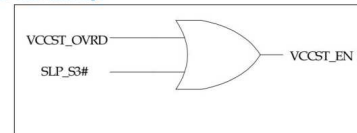
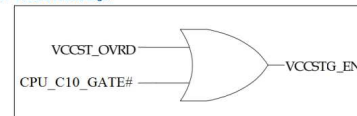
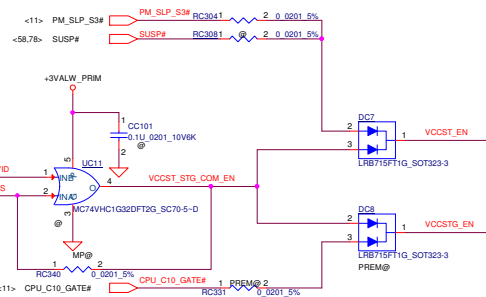


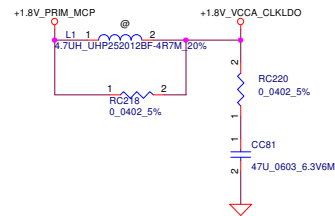
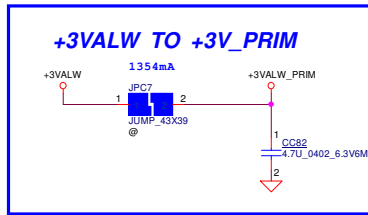
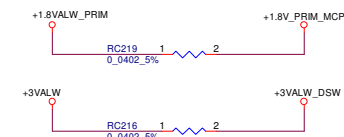
Figure 229. VCCSTG Enable Logic



VCCST/VCCSTG Enable

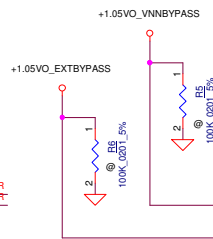
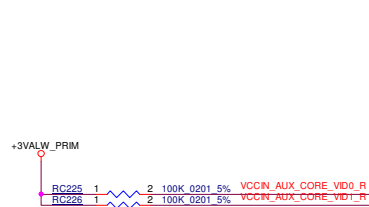
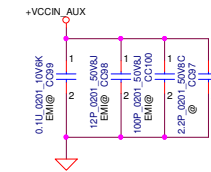
ICL have EC_VCCST_EN
check need it? or use syson/susp? 1210





Package size?

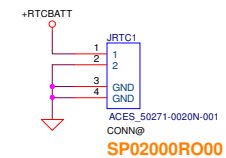
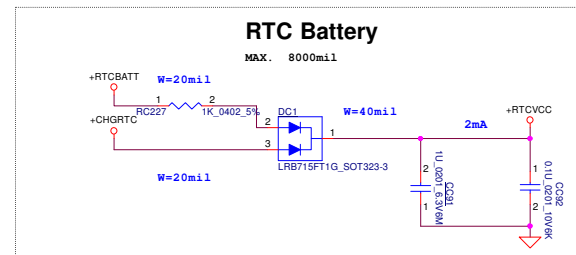
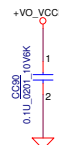
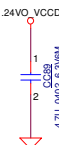
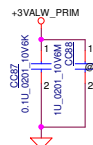
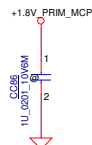
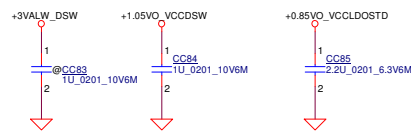
EMC CAPS-PLACE
< 5mm from SOC VCCIN_AUX



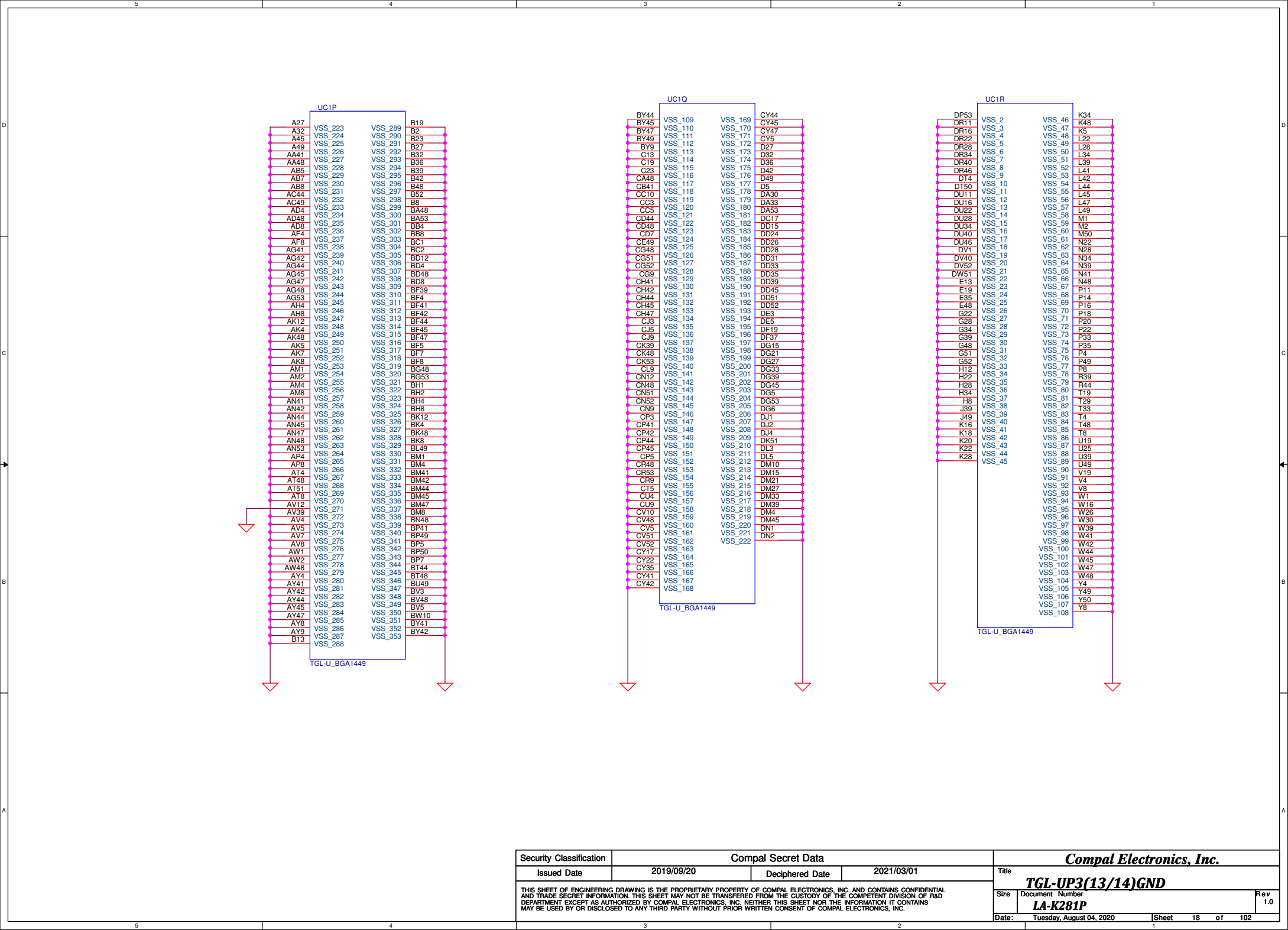
<7.43> VCCIN_AUX_CORE_ALERT#_R
<87> VNN_CTRL
<87> V1.05P_CTRL
<11.91> VCCIN_AUX_CORE_VID0_R
<11.91> VCCIN_AUX_CORE_VID1_R

<91> VSS_SENSE_VCCIN_AUX
<91> VCC_SENSE_VCCIN_AUX
VCCIN_AUX_VSSSENSE
VCCIN_AUX_VCCSENSE
VCC_VNNEXT_IP05_1
VCC_VNNEXT_IP05_2
VCC_V1P05EXT_IP05_1
VCC_V1P05EXT_IP05_2
GPP_B0/CORE_VID0
GPP_B1/CORE_VID1

NOTE:
576391-tgl-pch-lp-ads-vollof2-rev0p5
VCCPGPPR: Audio Power 3.3V, 1.5V, or 1.5V
Need to sync with codec VDDIO.
607872_TGL_UY_PDG_Rev0p5
When configured as 3.3V or 1.8V, VCCPGPPR can be merged directly with either VCCPRIM_IP8 or VCCPRIM_3P3 depending on their operating voltage.



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CFG	Description	Termination	Resistor
	Operation; No stall. - 9 = Stall		
CFG[0]	RSVD	None	
CFG[1]	RSVD	Pull-up to VCCIO	1K ohm
CFG[2]	RSVD	Pull-up to VCCIO	1K ohm
CFG[3]	RSVD	Pull-up to VCCIO	1K ohm
CFG[4]	eDP enable Strap: - 1 = Disabled. - 0 = Enabled.	Pull-up to VCCIO / Pull-down- Platform design dependent	1K ohm
CFG[6:5]	RSVD	None	
CFG[7]	PEG deferred link training	Pull-up to VCCIO / Pull-down- Platform design dependent	1K ohm
CFG[8]	RSVD	None	
CFG[11:9]	RSVD	Pull-up to VCCIO	1K ohm
CFG[13:12]	RSVD	None	
CFG[14]	PEG60 Lane Reversal: - 1 (Default) Normal - 0 - Reversed	Pull-up to VCCIO / Pull-down- Platform design dependent	1K ohm
CFG[1 7:15]	RSVD	None	

CFG4
Display port presence strap
LOW : Enable
An external display port device is connected to the embedded displayport
HIGH : Disable
No physical display port attached to embedded display port

0109 remove ES1@ componet



S IC FH8069004531602 SRK08 B1 3G ABO !
SRK08@
SA0000DTV50



S IC FH8069004531301 SRK05 B1 2.4G ABO !
SRK05@
SA0000DTU30



S IC FH8069004530104 SRK02 B1 2.8G ABO !
SRK02@
SA0000DTT30



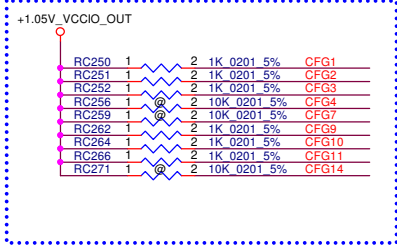
PCB@
PCB GH4FT LA-K281P LS-K281P/J732P
DAZ36W00101



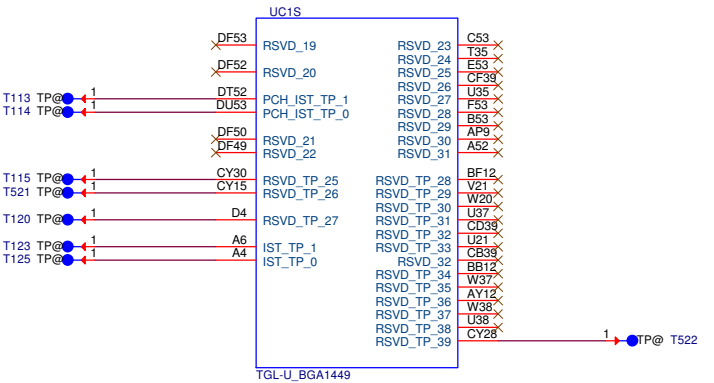
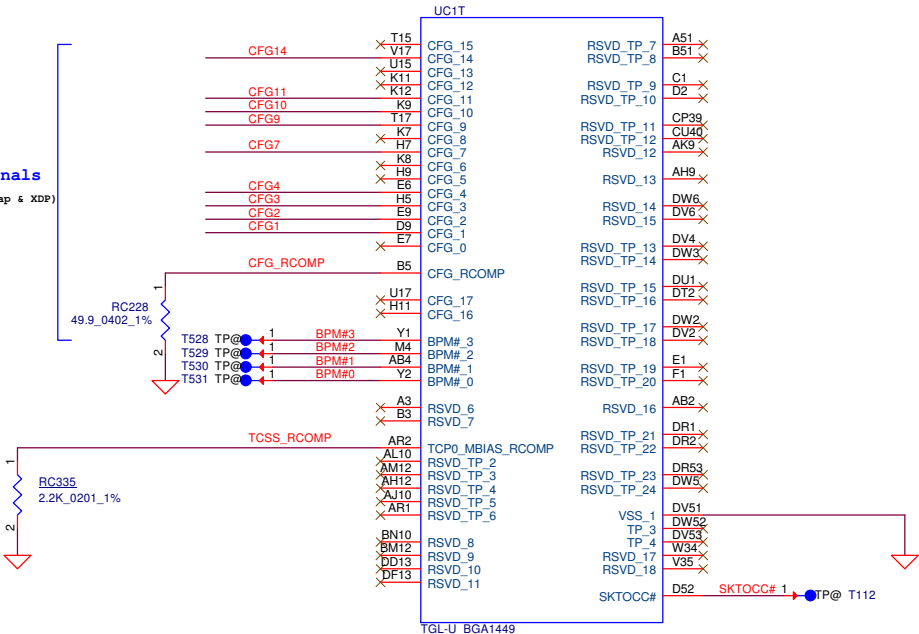
X4E@
SMT EMC EE UMA MB AK281 GH4FT
X4EANQBOL01



HDMI LOGO LOGO@
RO0000003HM



CFG Signals
(For Strap & XDP)



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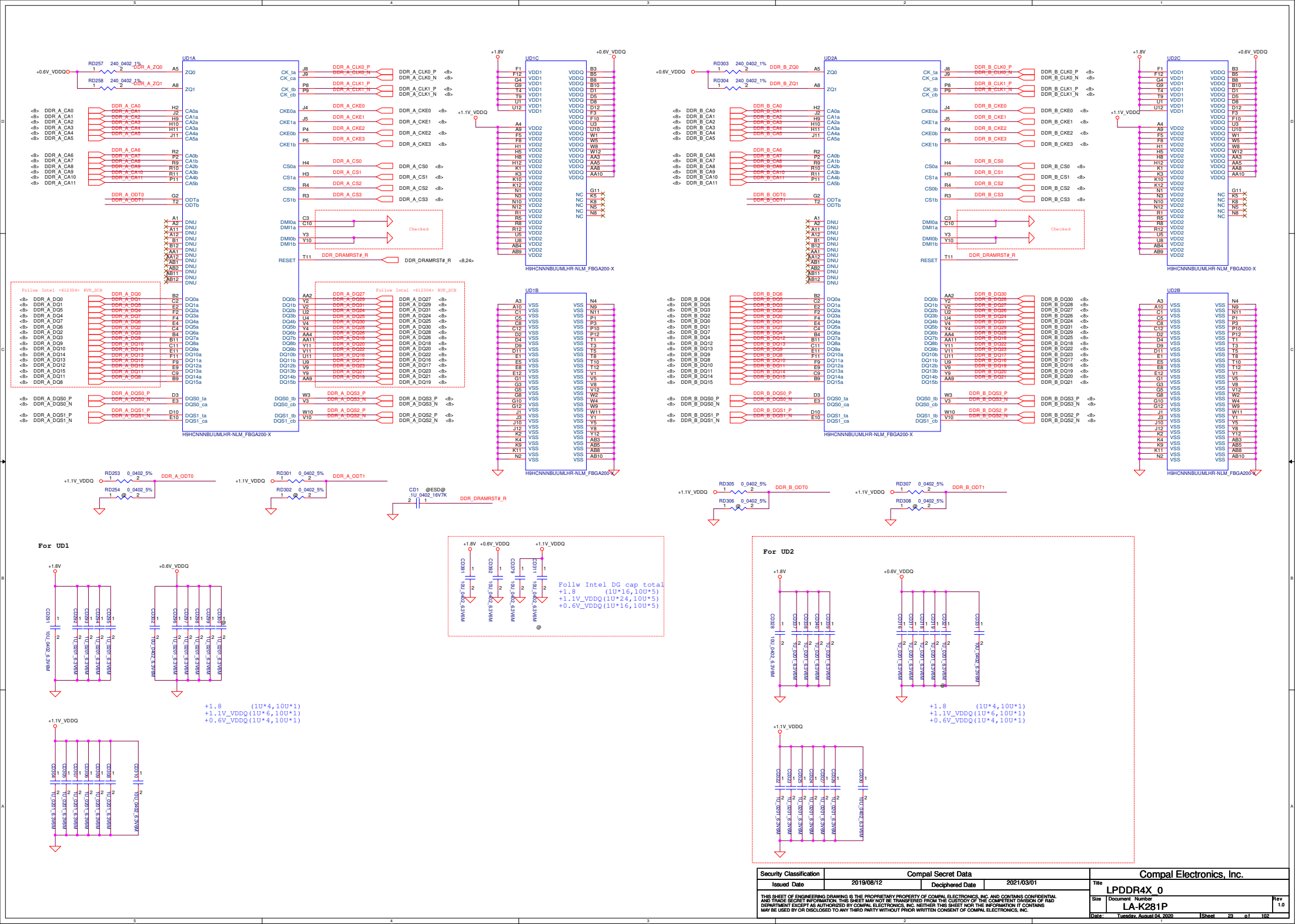
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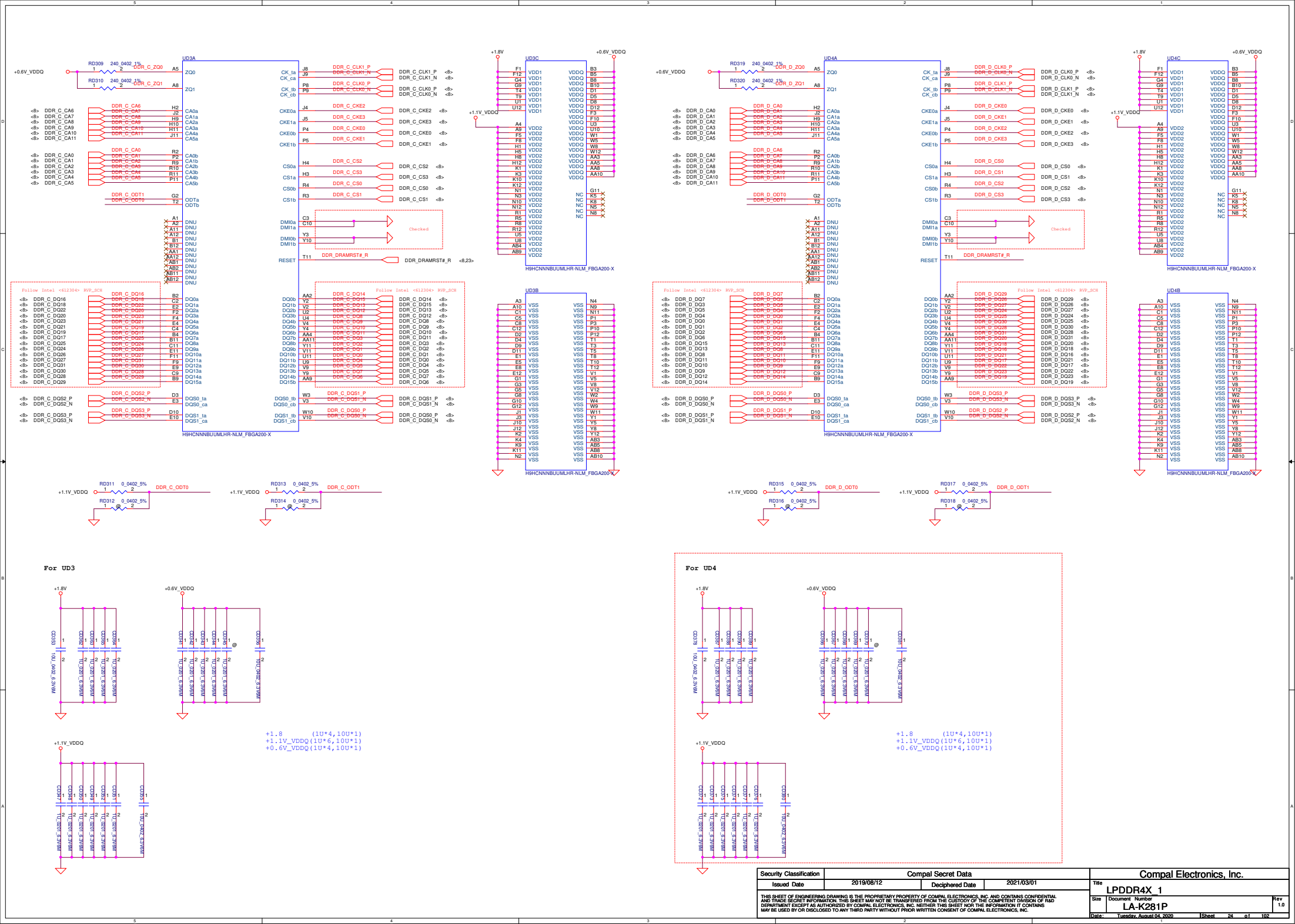


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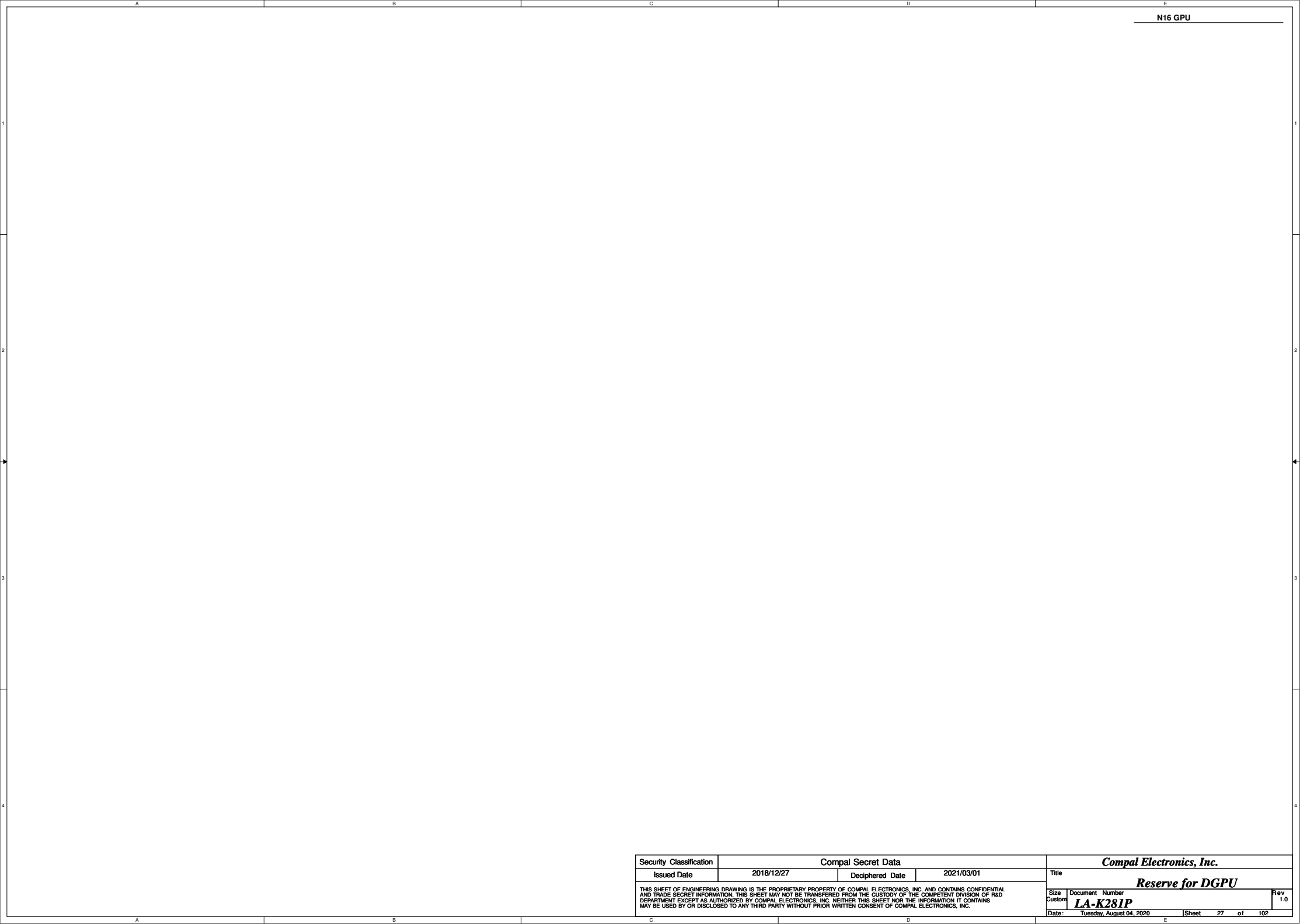




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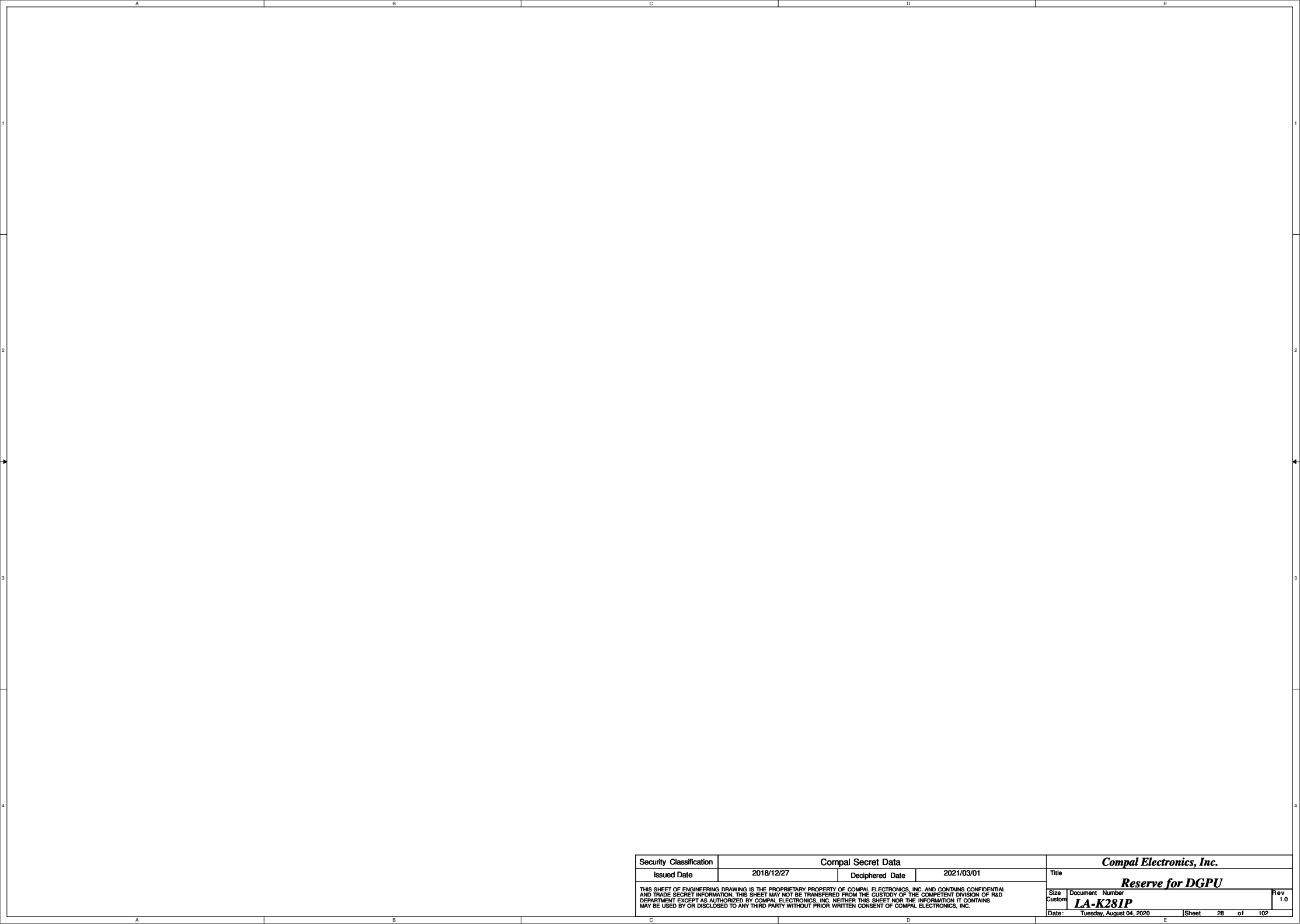


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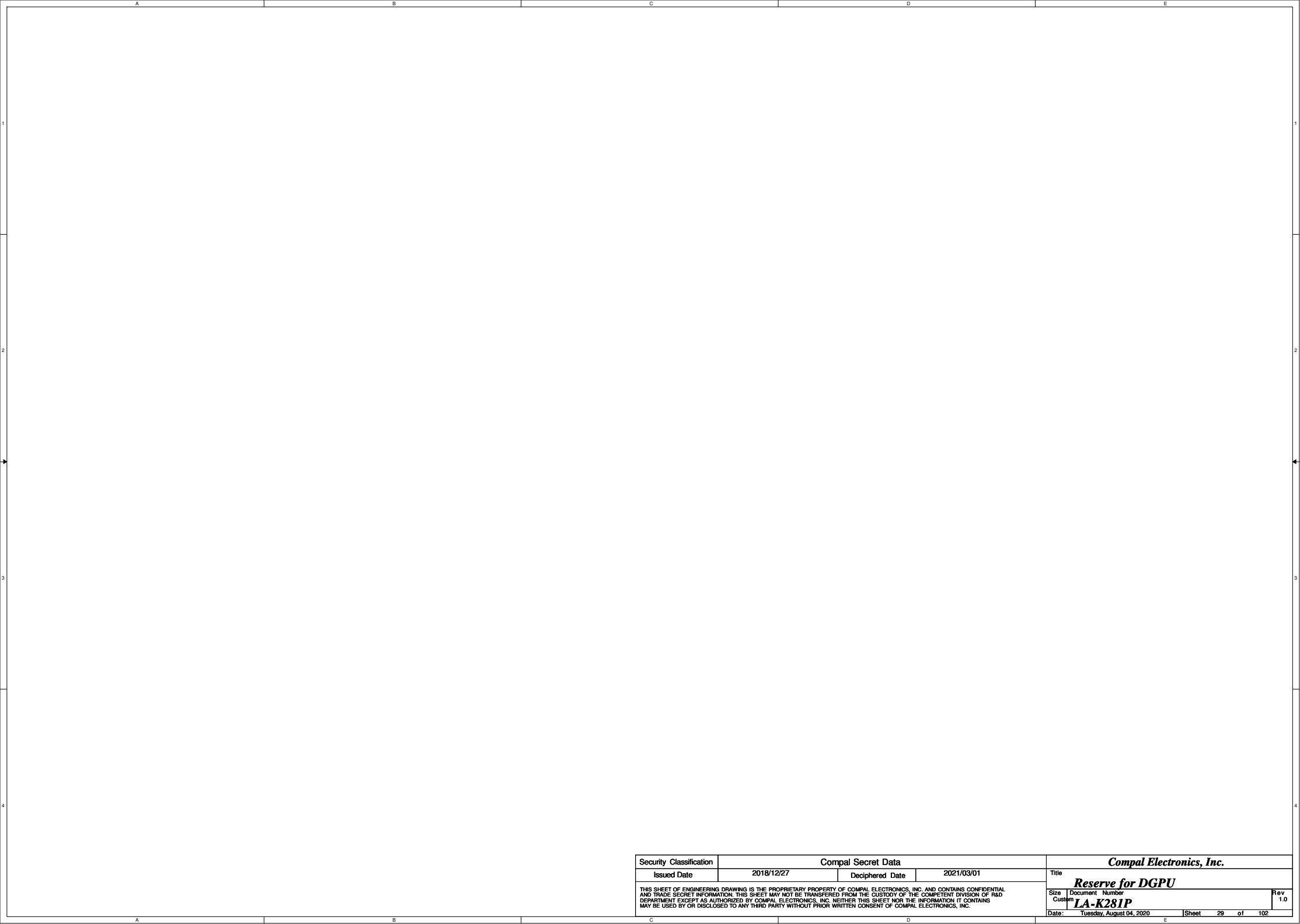


N16 GPU

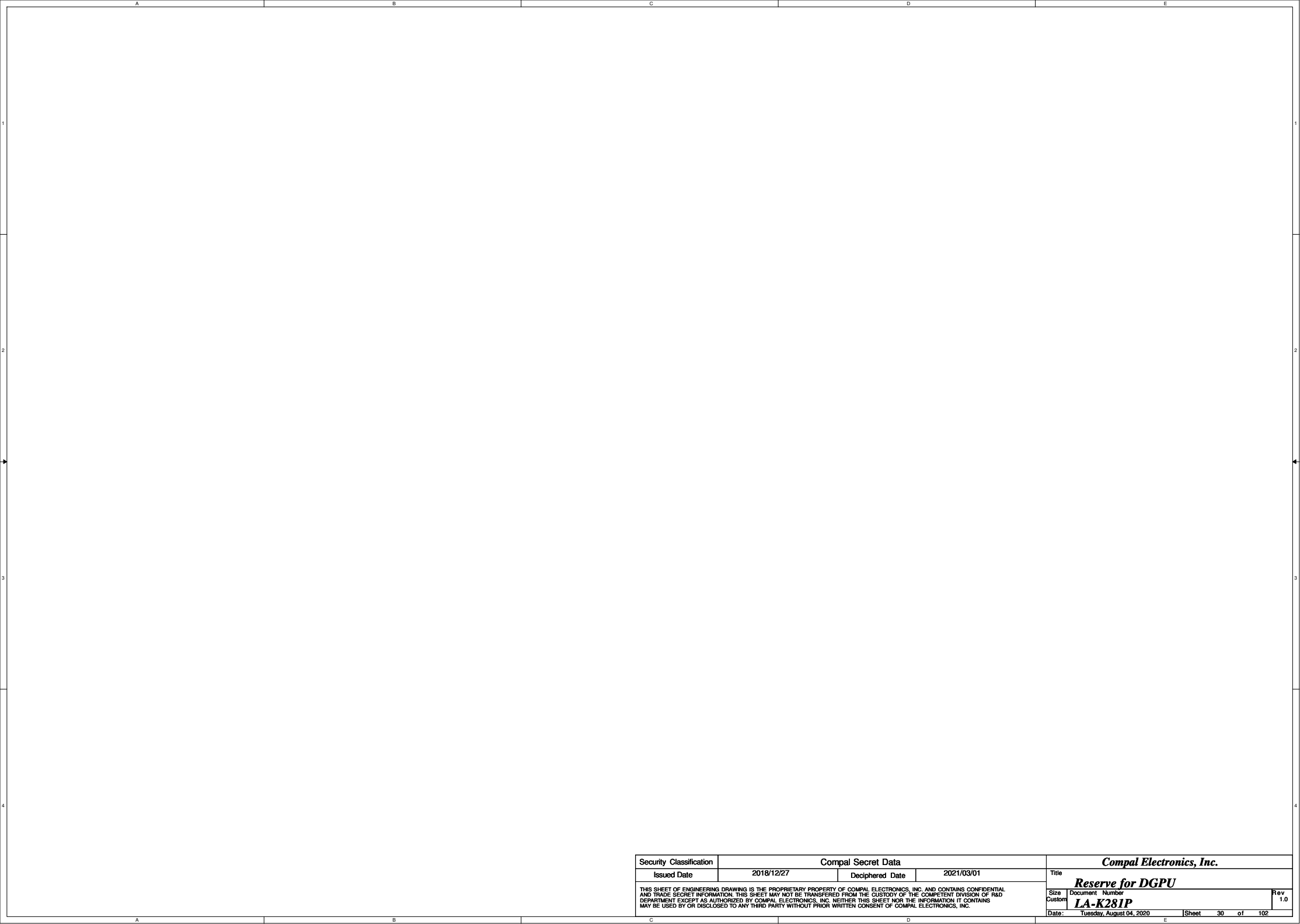
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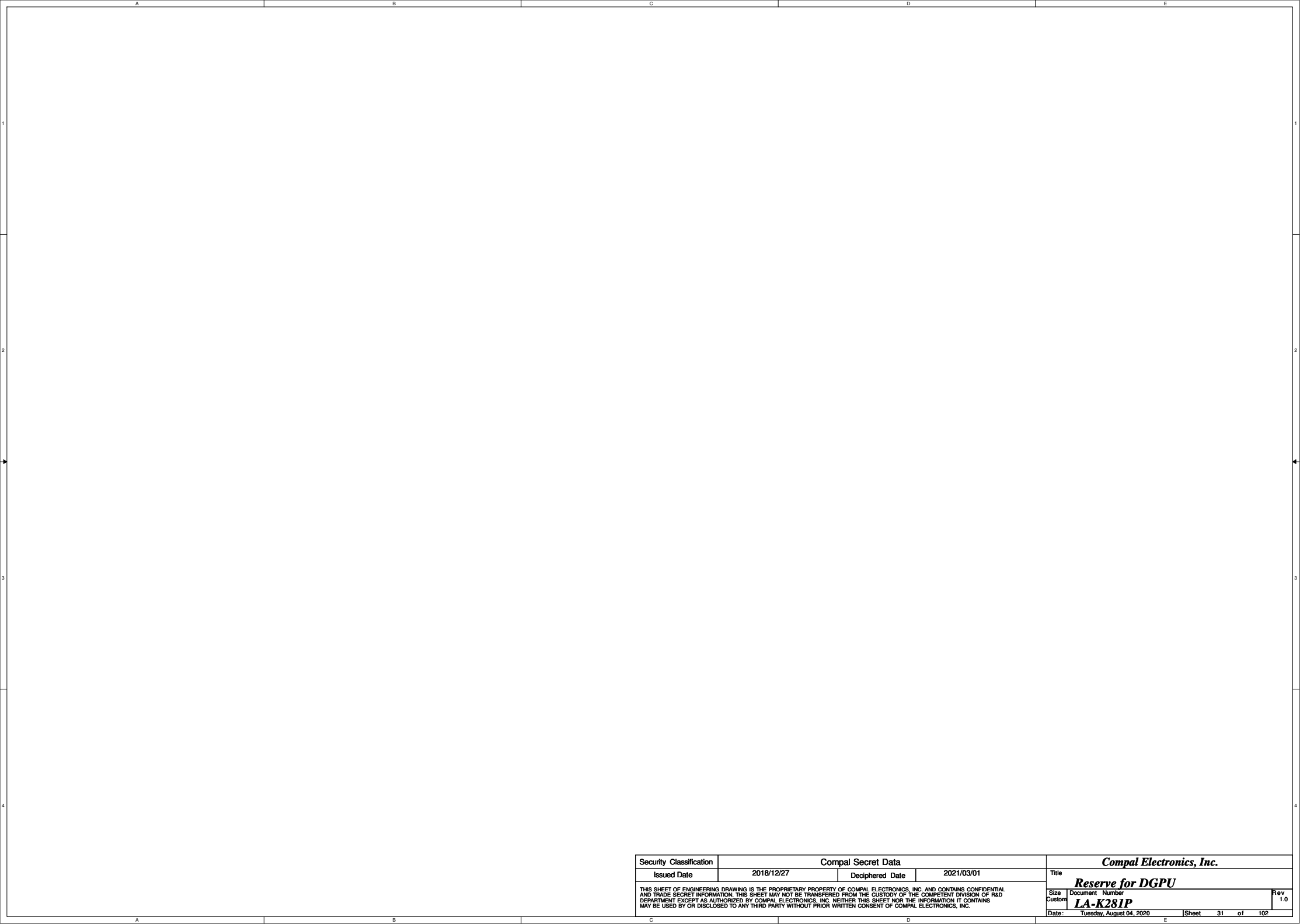
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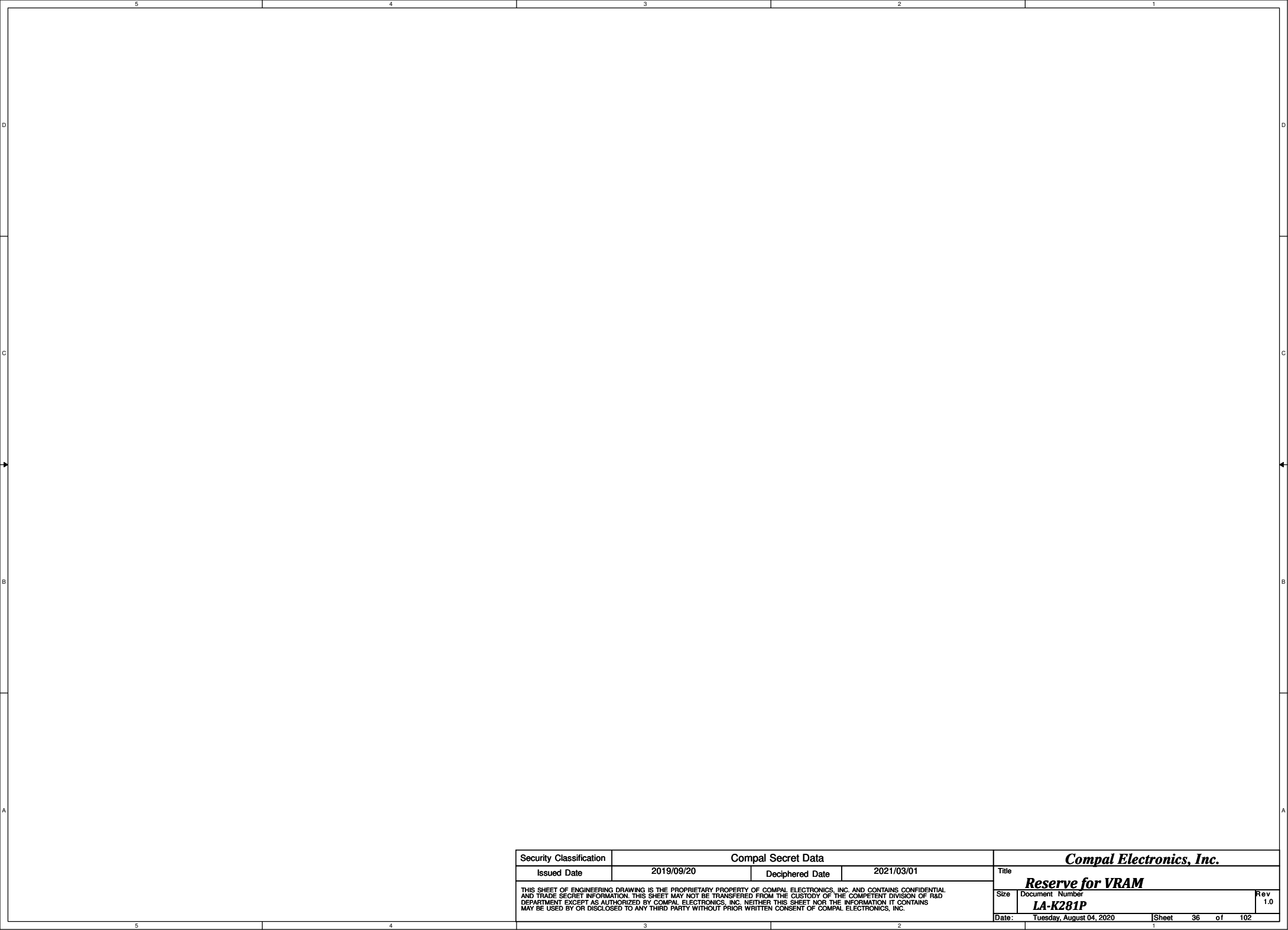
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					LA-K281P		
					1.0		
Date:					Tuesday, August 04, 2020		Sheet 34 of 102



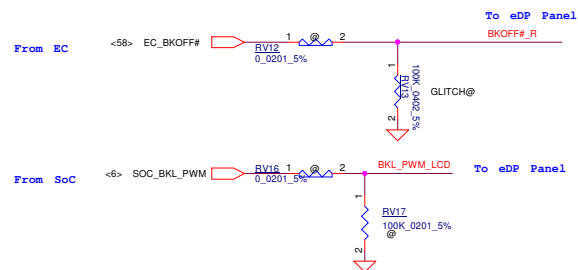
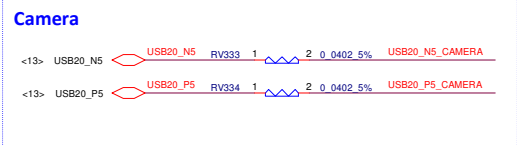
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Date:					Tuesday, August 04, 2020				
Sheet					36 of 102				

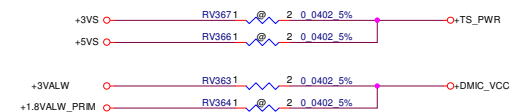
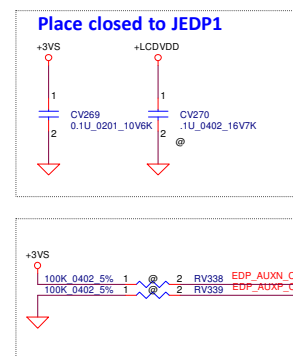
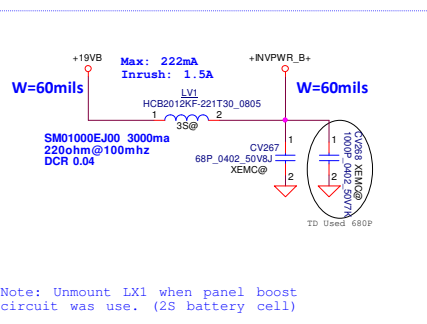


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				Date:	
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				Sheet 37 of 102	

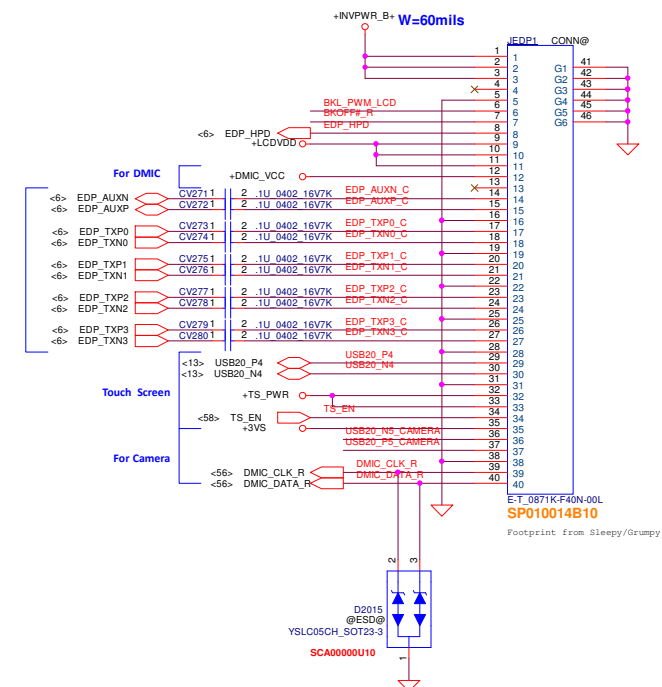


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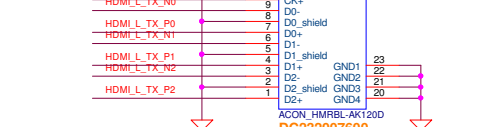
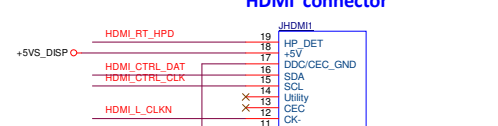
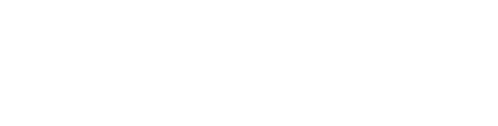
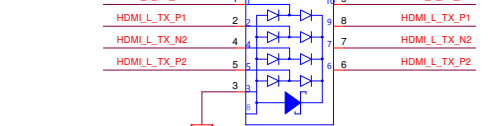
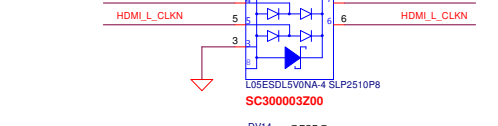
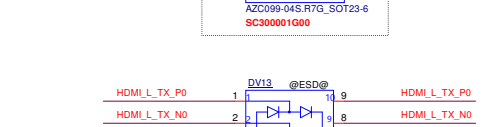
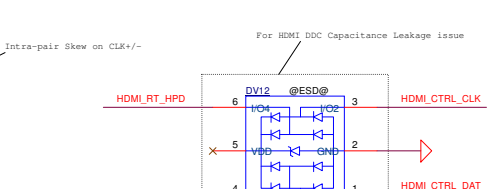
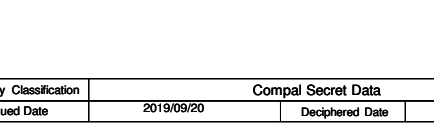
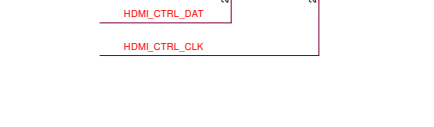
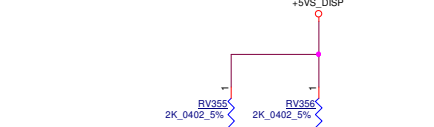
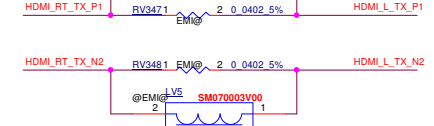
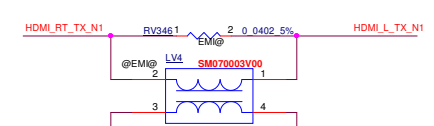
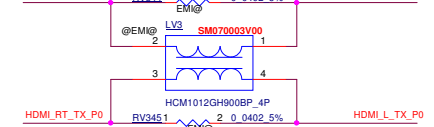
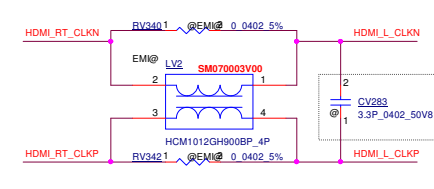
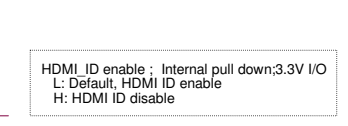
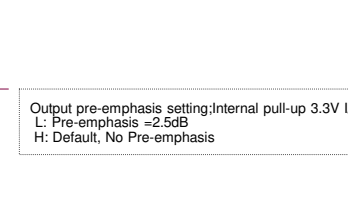
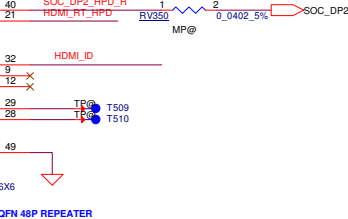
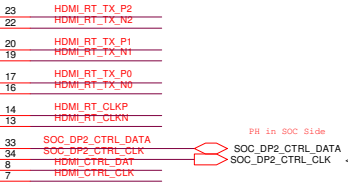
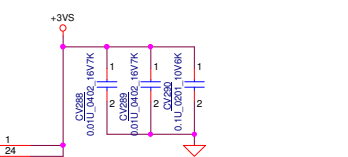
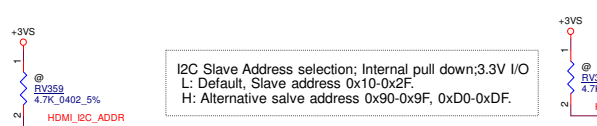
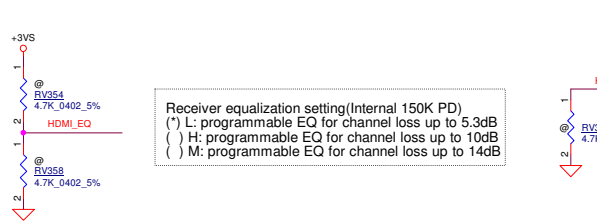
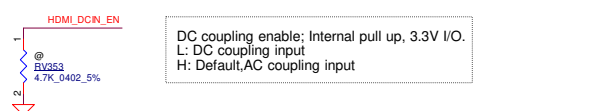
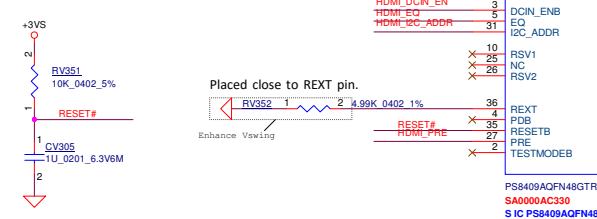
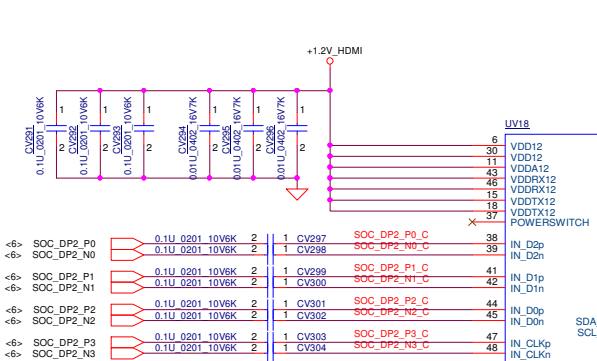
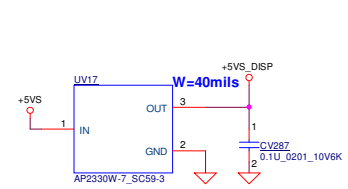
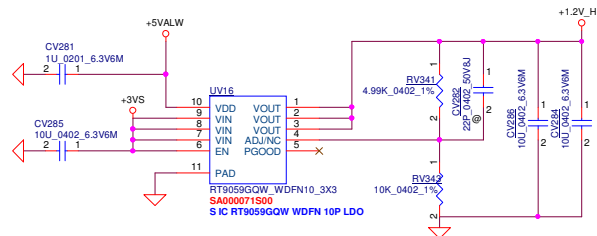
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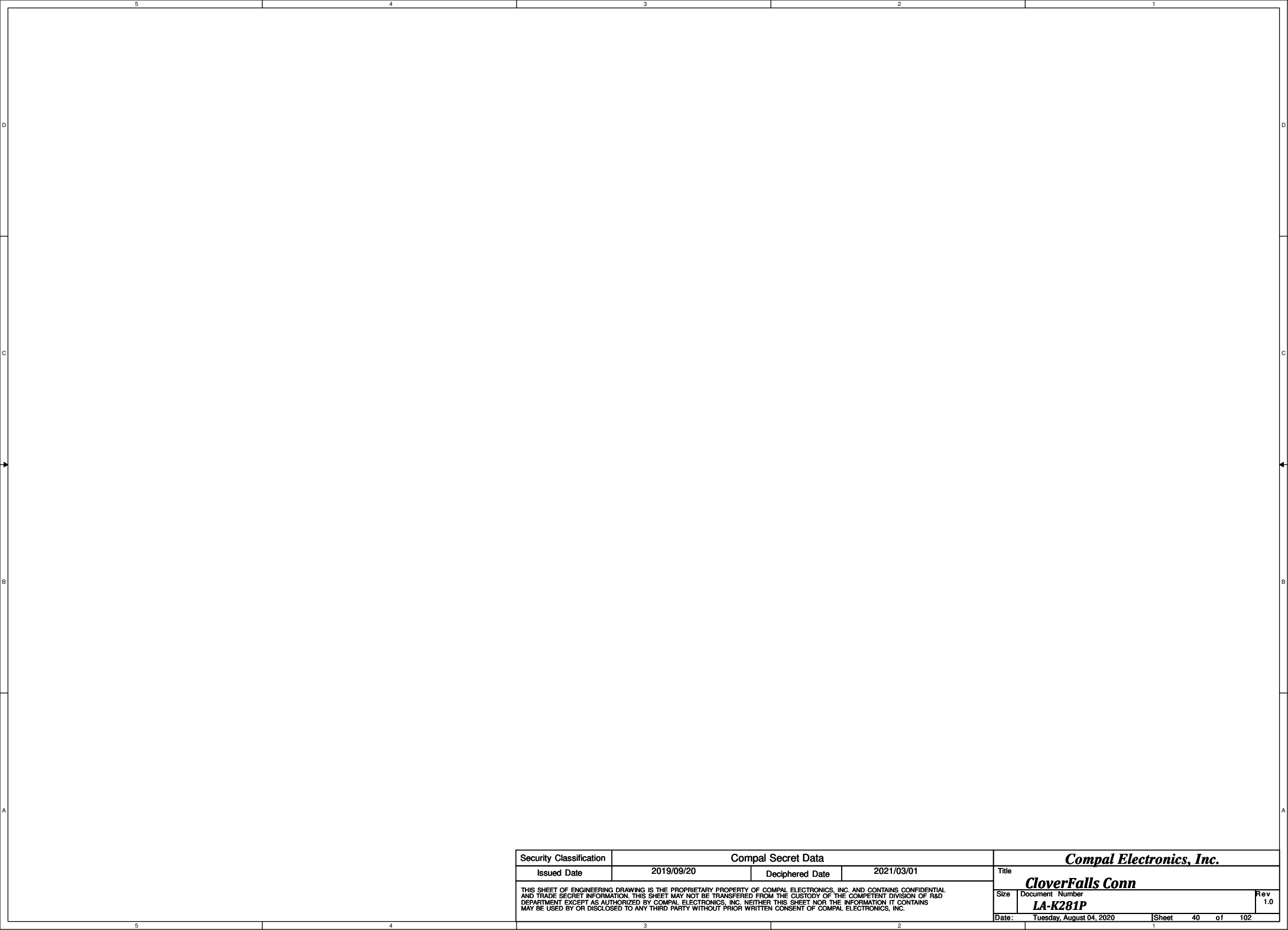
LED PANEL Conn.



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						Size	Document Number	Rev
						LA-K281P		1.0
						Date:	Tuesday, August 04, 2020	Sheet 40 of 102

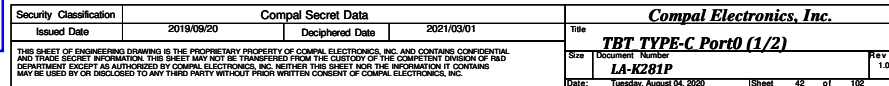


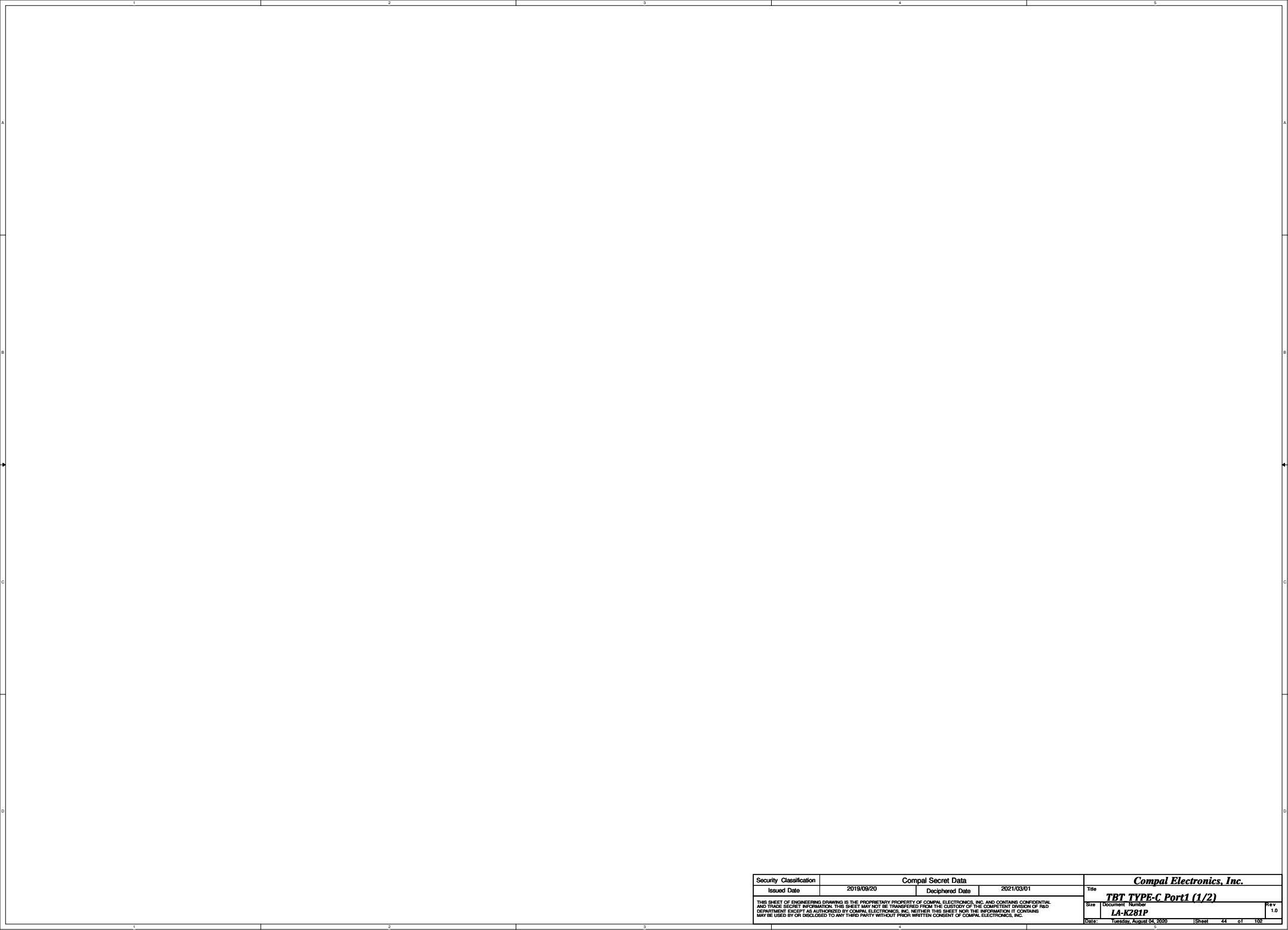
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						Size	Document Number		Rev			
						LA-K281P					1.0	
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											Sheet	41 of 102

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RDS(Typ) : 70 mohm
V drop : 0.026 V

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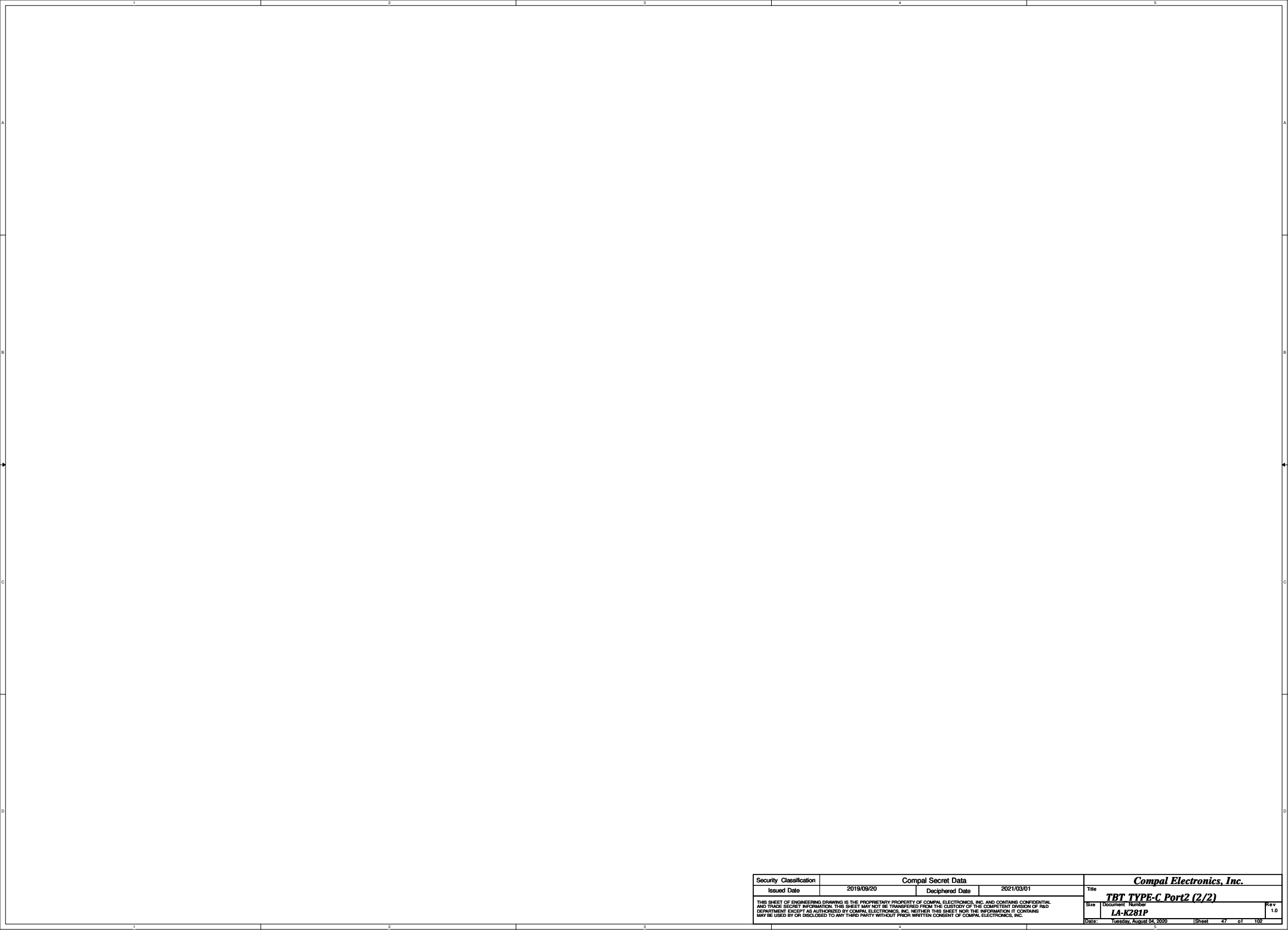
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				Size	Document Number
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								Size		Document Number		Rev	
								LA-K281P		1.0			
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								Date:		Tuesday, August 04, 2020		Sheet 46 of 102	

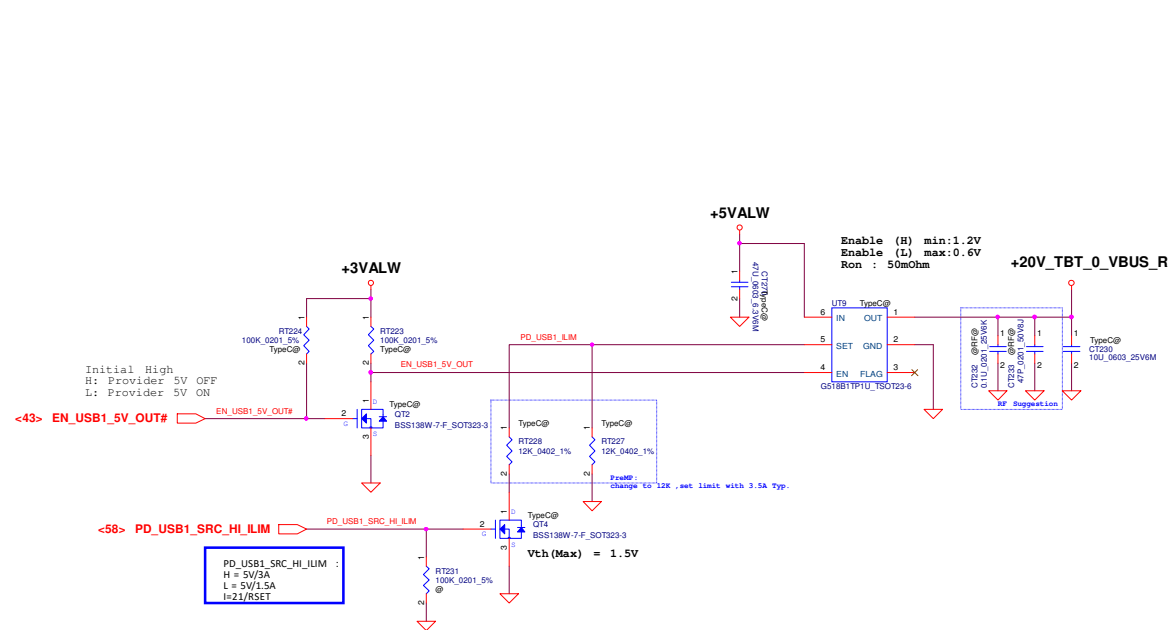


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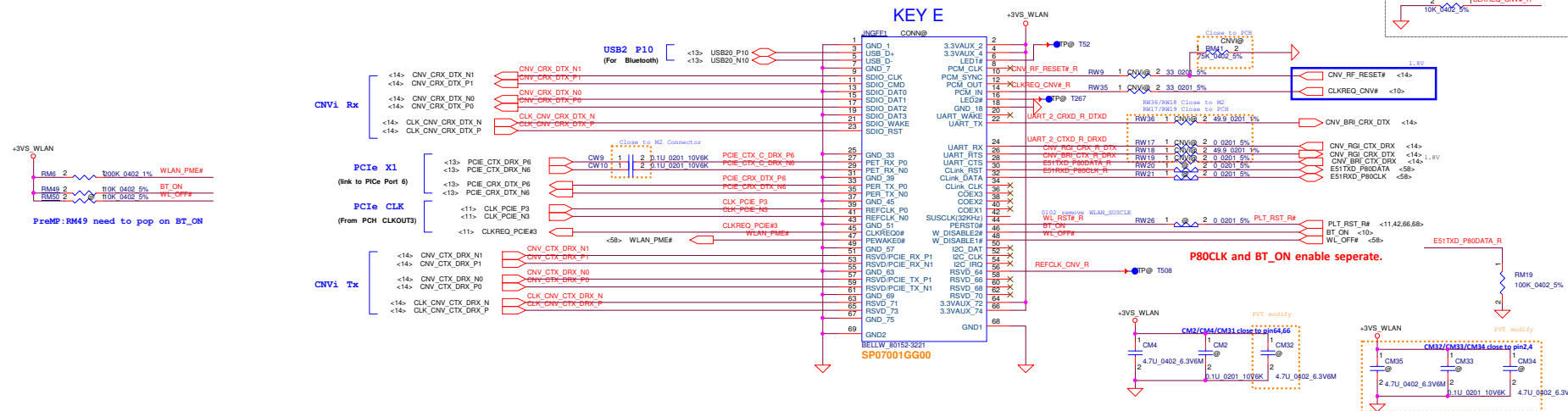
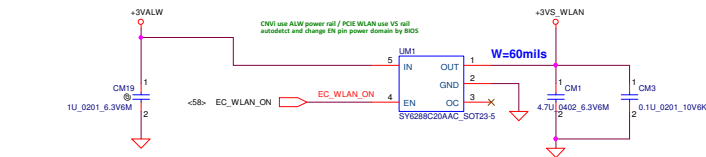
MB_USB3.1 TypeC Conn. (Power Path)



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					LAN-RTL8111H		
					Size	Document Number	Rev
					LA-K281P		
					Rev 1.0		
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					Size	Document Number		Rev
						LA-K281P		1.0
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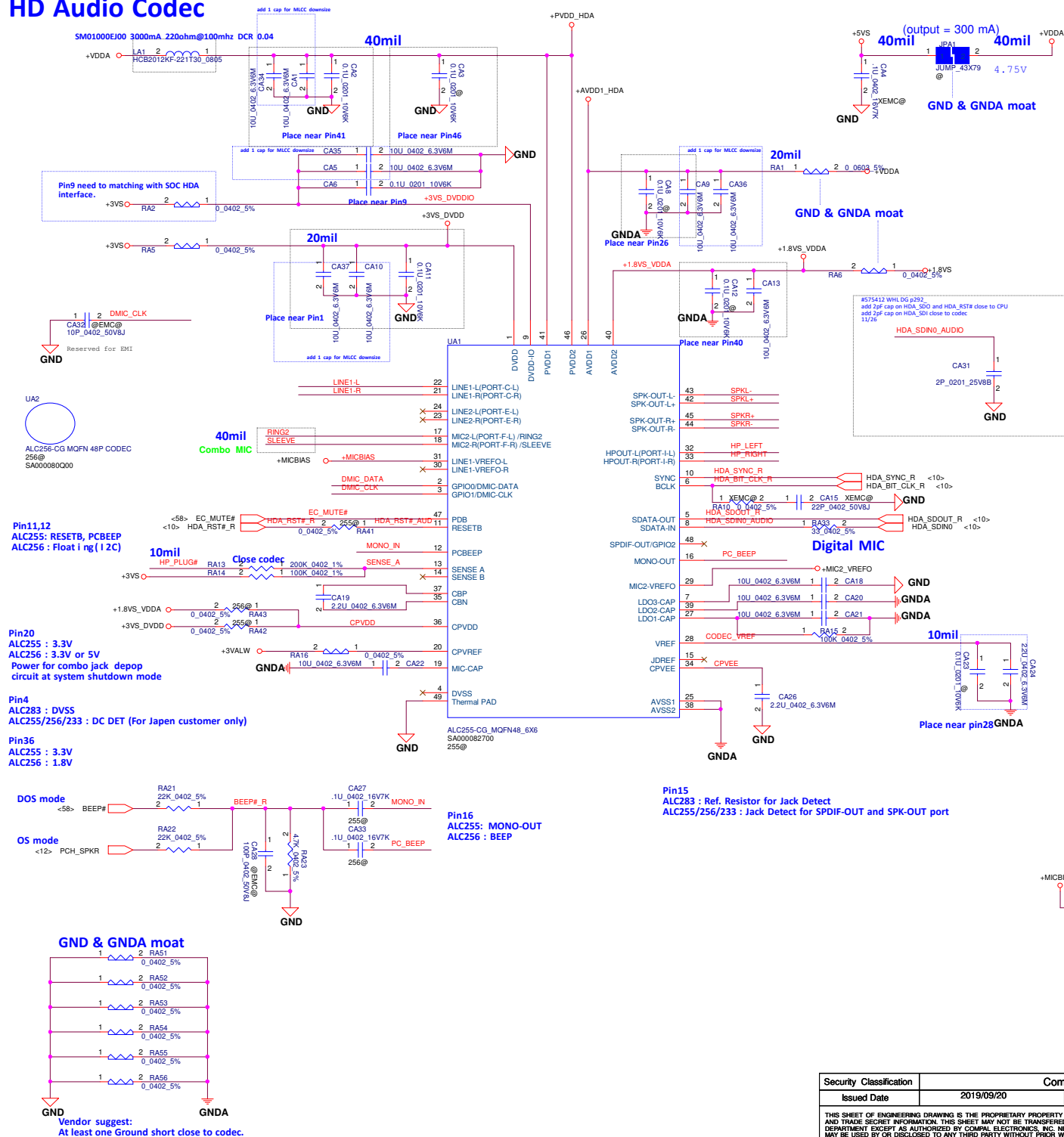
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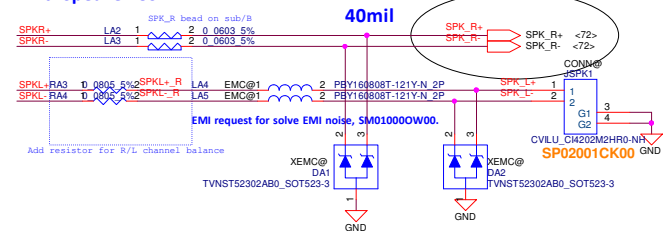


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								LA-K281P				1.0	
								Date:		Tuesday, August 04, 2020		Sheet 55 of 102	

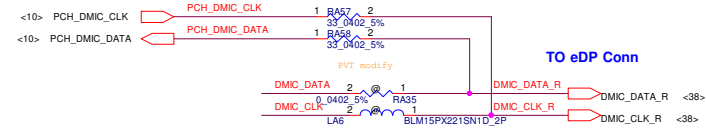
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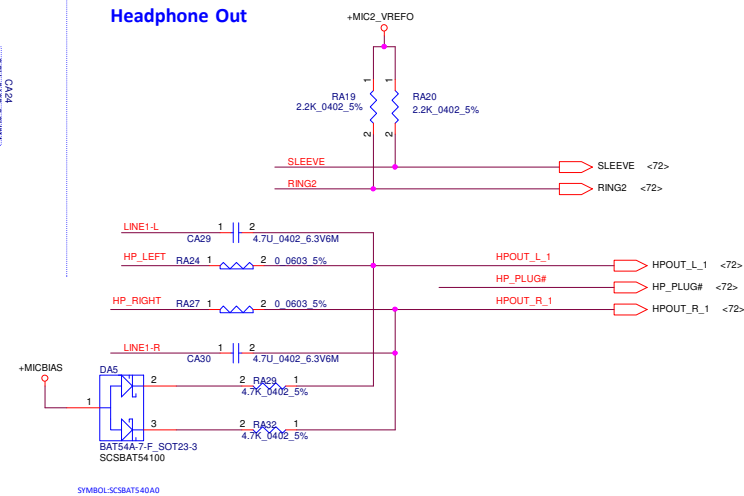
Int. Speaker Conn.



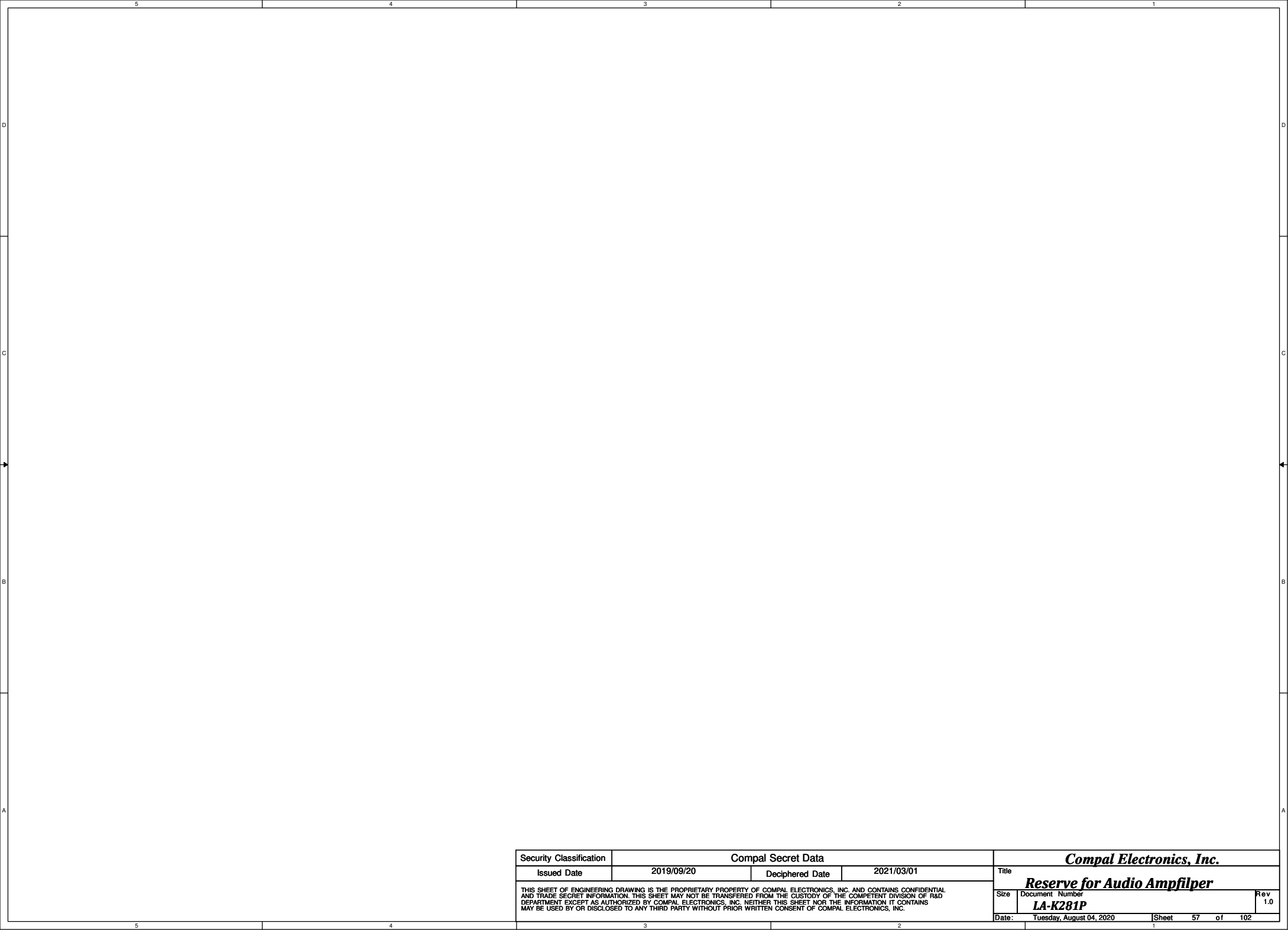
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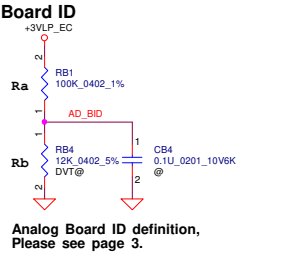
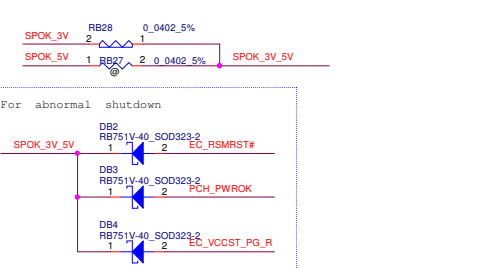
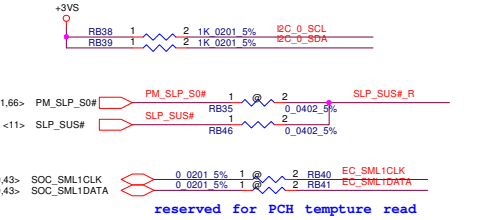
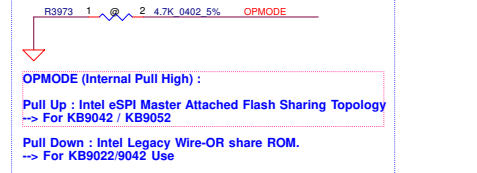
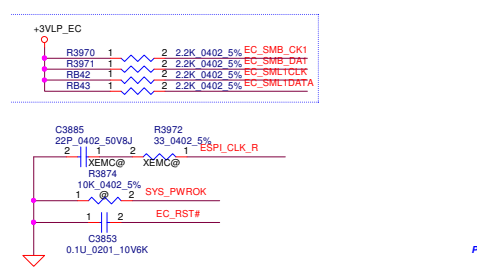
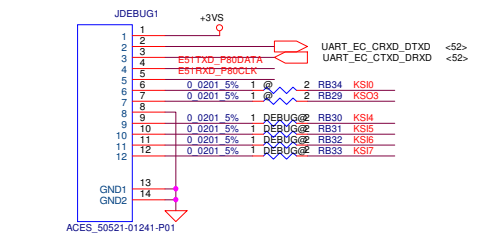
Headphone Out



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				LA-K281P			1.0
				Date:	Tuesday, August 04, 2020	Sheet	56 of 102



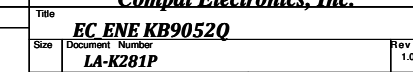
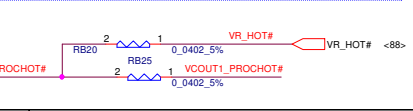
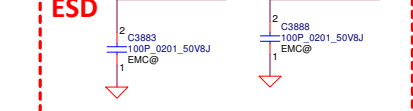
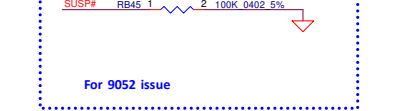
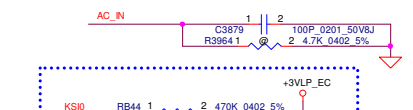
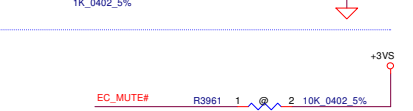
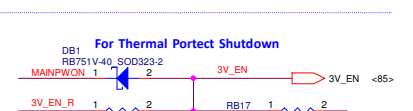
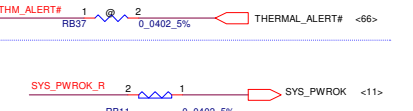
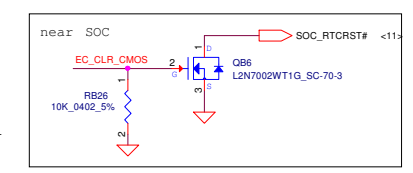
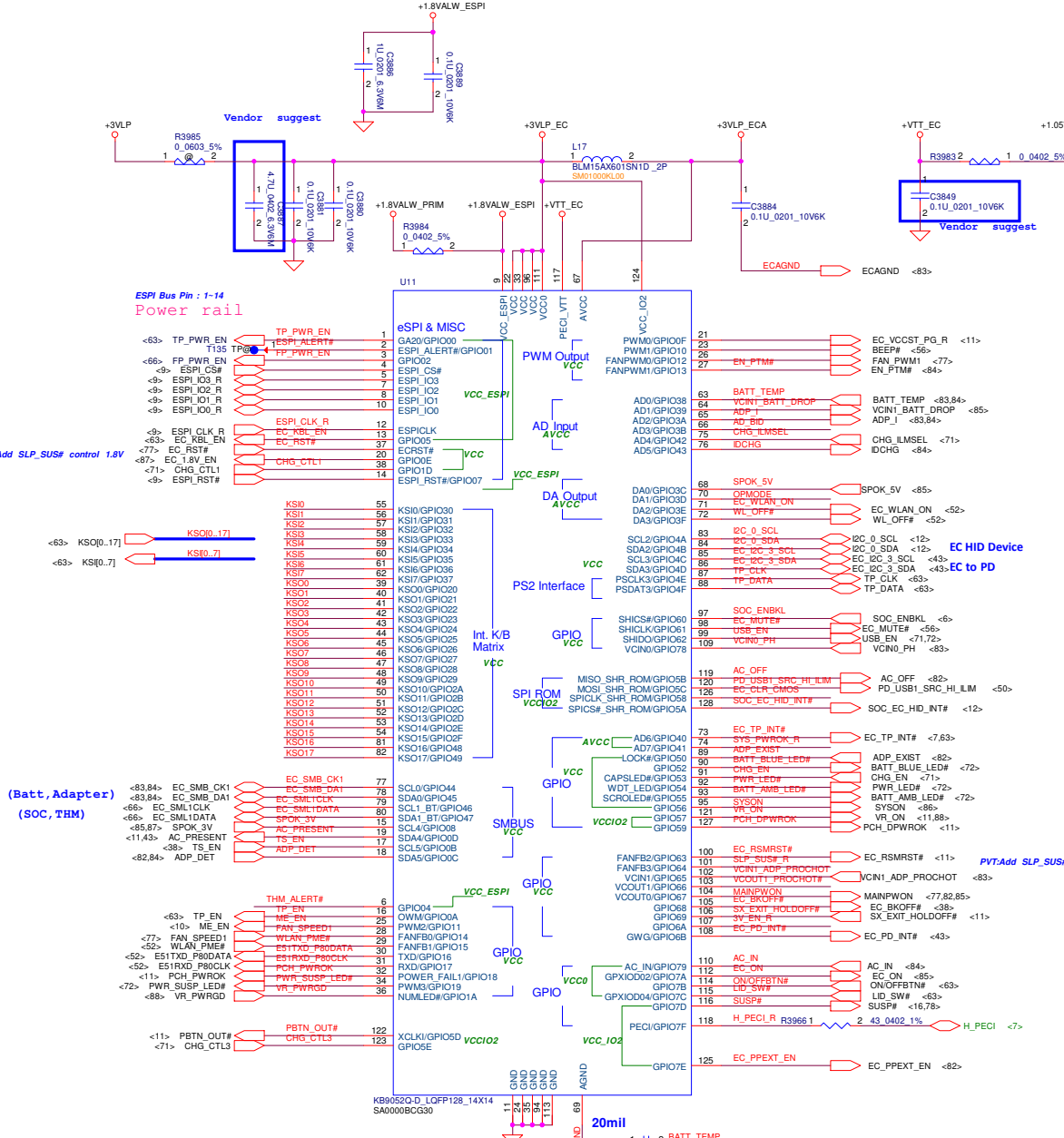
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					Size	Document Number	Rev
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IO pin groups v.s Power planes:

Power plane	Voltage	Pin#	Output Pin Power Rail	Input Pin VIH/VIL
VCC0	3.3V~2.0V(min) for PLC operation and data retention	110, 112, 114, 115	Push-pull @ VCC0 Open-drain up to 5V	ref. to VCC0
VCC	3.3V only	15-43	Push-pull @ VCC Open-drain up to 5V	ref. to VCC
VCC_ESPI	1.8V	1-14	Push-pull @ VCC_ESPI Open-drain up to VCC_ESPI	ref. to VCC_ESPI
AVCC	3.3V only	63-76 (102~109)	Push-pull @ AVCC Open-drain up to 5V	ref. to AVCC
VCC_I02	1.8V or 3.3V	116, 118-128	Push-pull @ VCC_I02 Open-drain up to 5V	ref. to VCC_I02
PECL_VTT	External applied Vtt	117		

Note: pin-109 (VCIN0) can be programmable internally connected to ADC ch8 (ADC8) and pin-102 (VCINT) to ch9 (ADC9) by setting ADEN2[5:4]. If so, the voltage level on these two pins should not be higher than AVCC to prevent leakage.

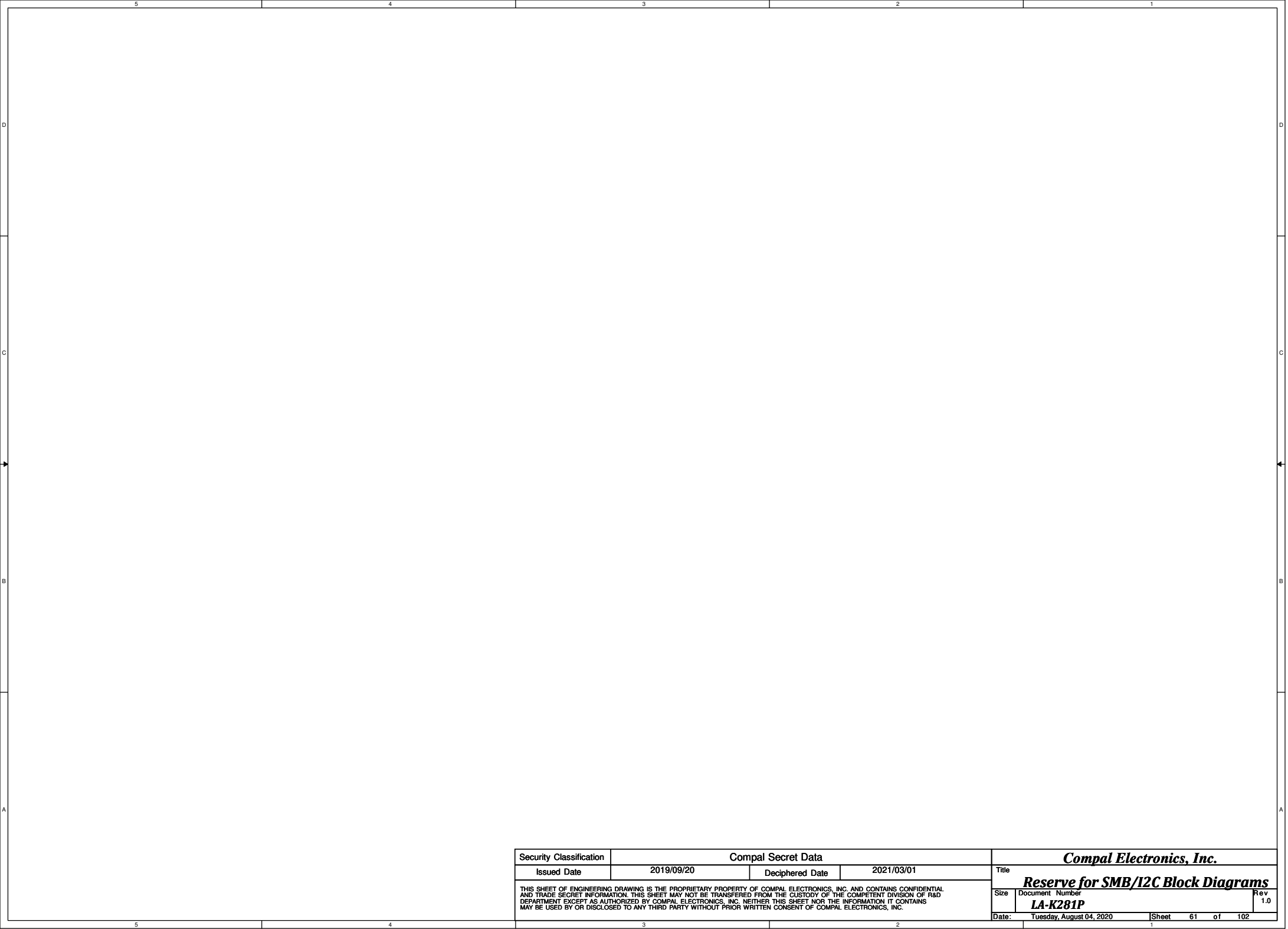




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								LA-K281P				1.0	
								Date:		Tuesday, August 04, 2020		Sheet 59 of 102	



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								Size		Document Number		Rev	
								LA-K281P		1.0			
								Date:		Tuesday, August 04, 2020		Sheet 60 of 102	

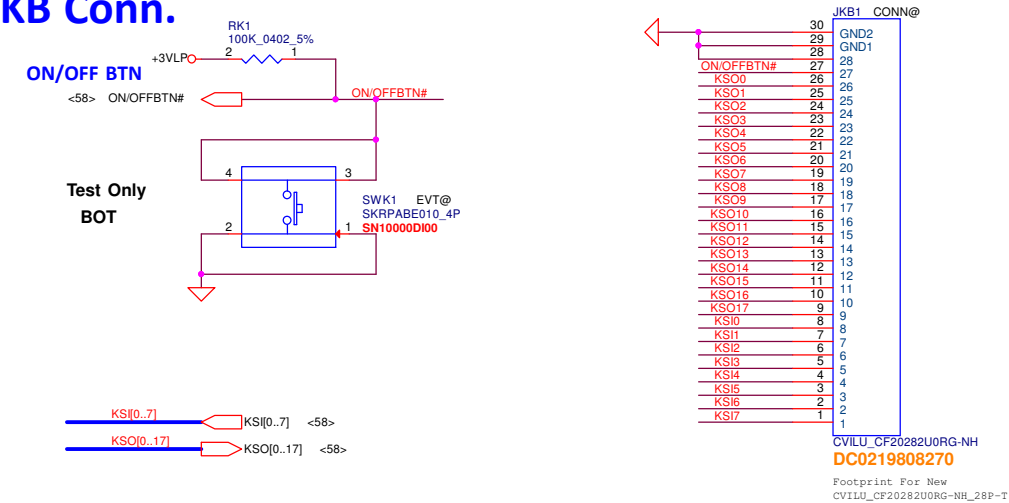


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								LA-K281P		1.0			
								Date:		Tuesday, August 04, 2020		Sheet 61 of 102	

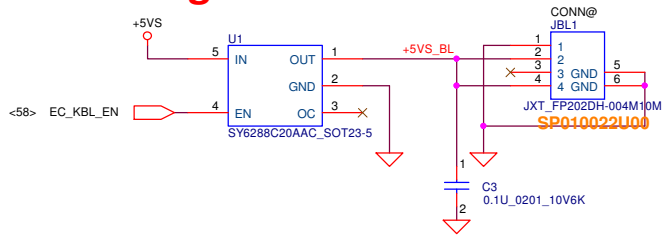


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				Sheet	62 of 102
				Rev	1.0

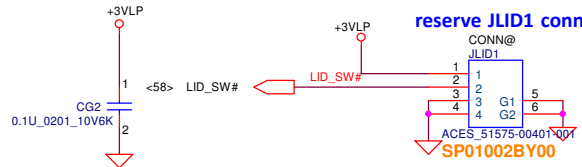
KB Conn.



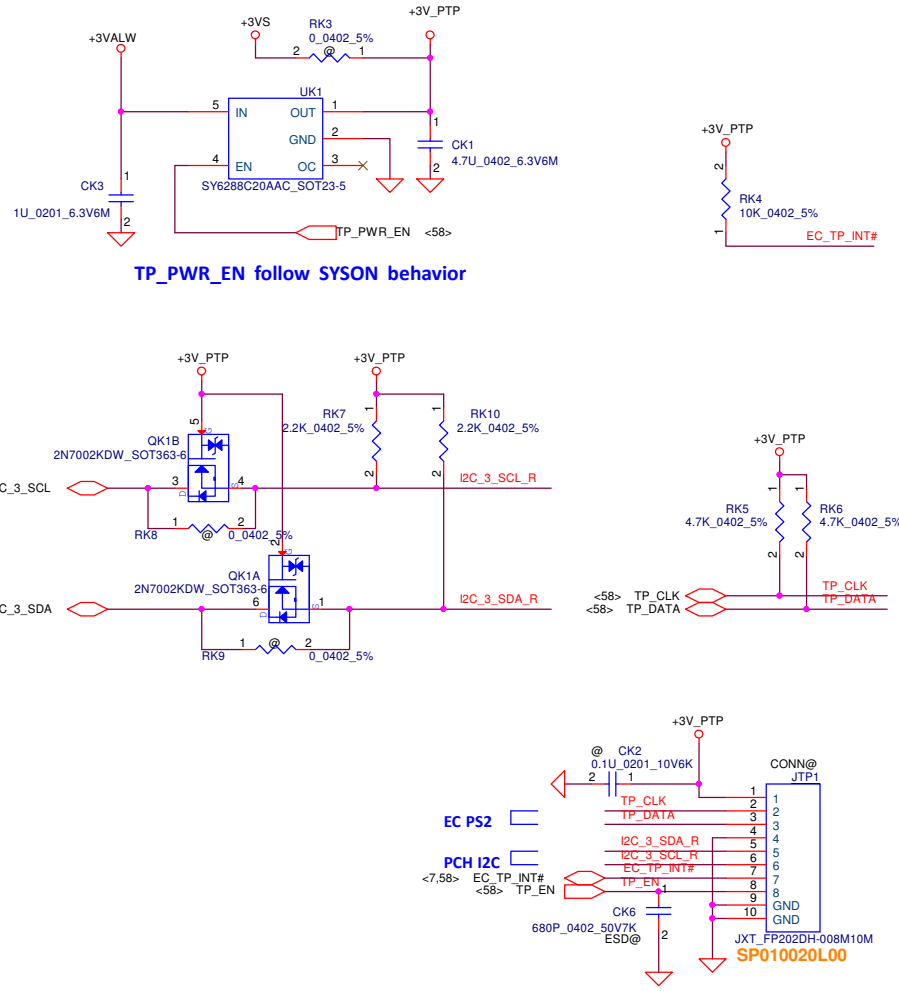
KB BackLight



Lid Switch



TP/B Conn.



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Size		Document Number		Rev	
Custom		LA-K281P		1.0	
Date:		Tuesday, August 04, 2020		Sheet 63 of 102	

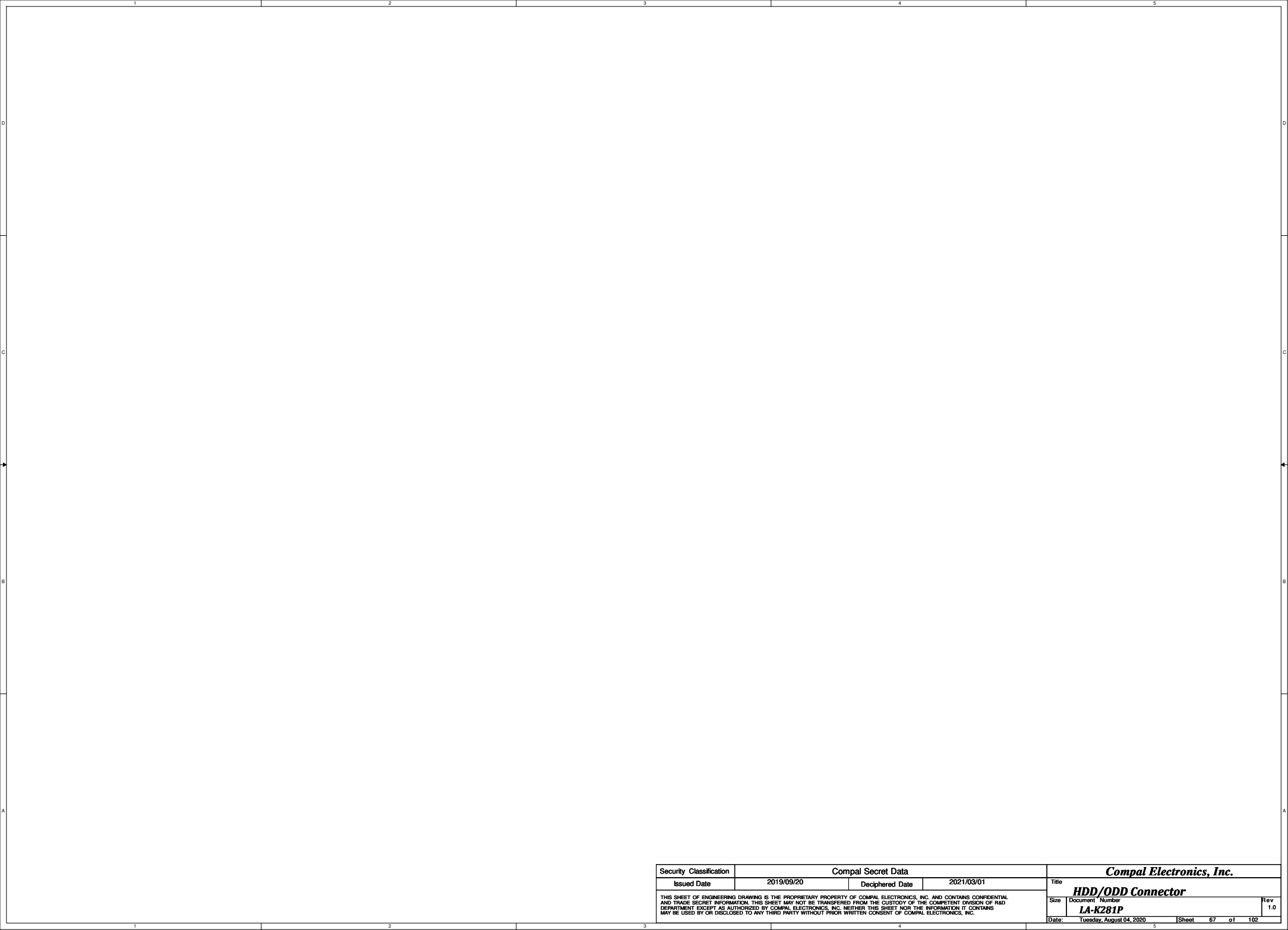


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					LA-K281P		1.0
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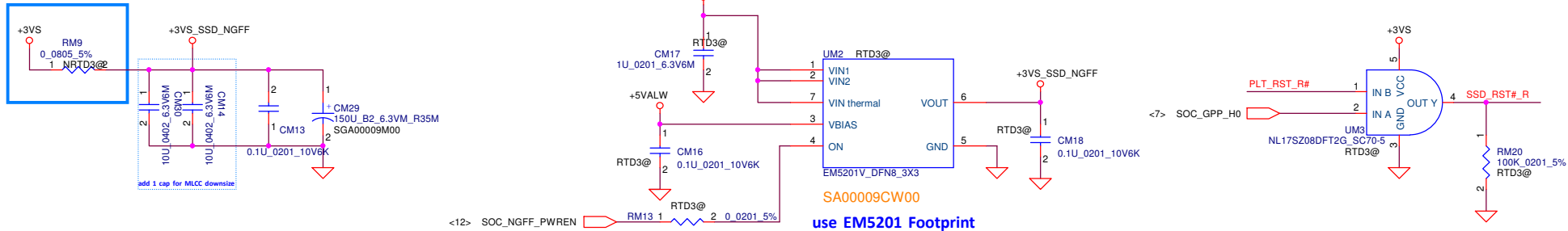
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					Size Document Number		Rev
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				Document Number LA-K281P	
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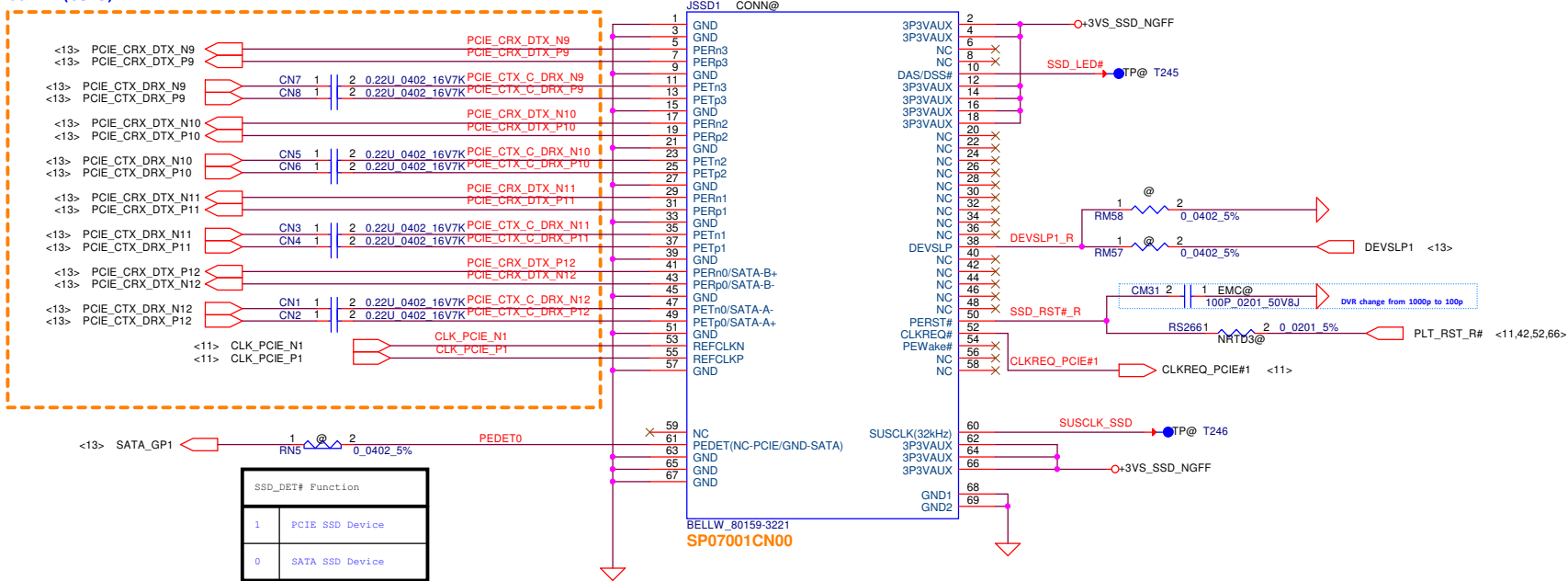


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2019/09/20		2021/03/01		LA-K281P	
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M.2 SSD



KEY M



SSD_DET# Function	
1	PCIe SSD Device
0	SATA SSD Device

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				LA-K281P	
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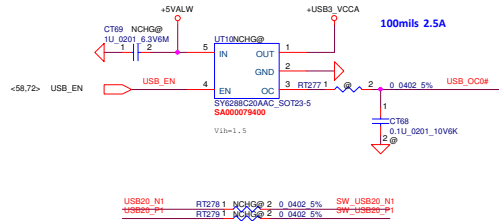


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								LA-K281P				1.0	
								Date:		Tuesday, August 04, 2020		Sheet 69 of 102	

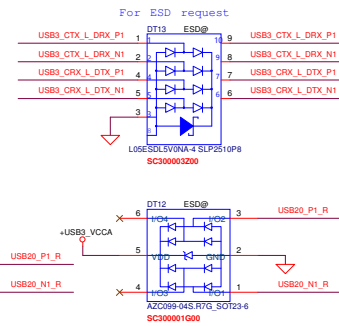
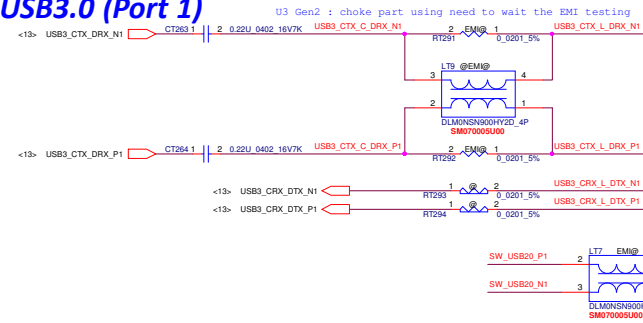
+3VS TO +3VS_CARD

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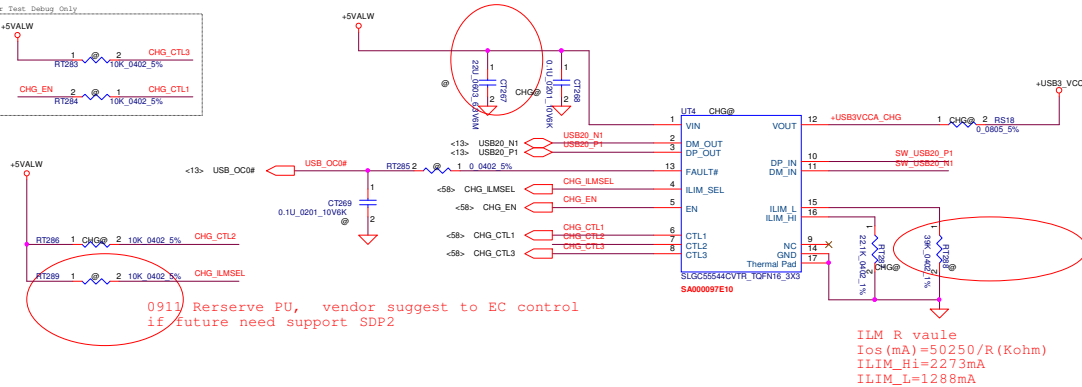
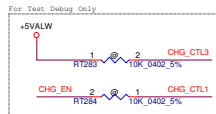
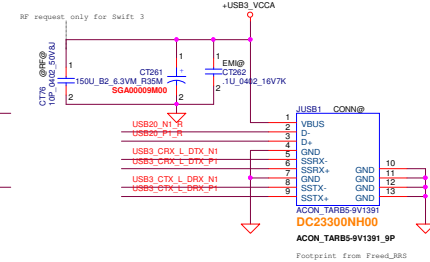
Non-Charger Co-lay



USB3.0 (Port 1)



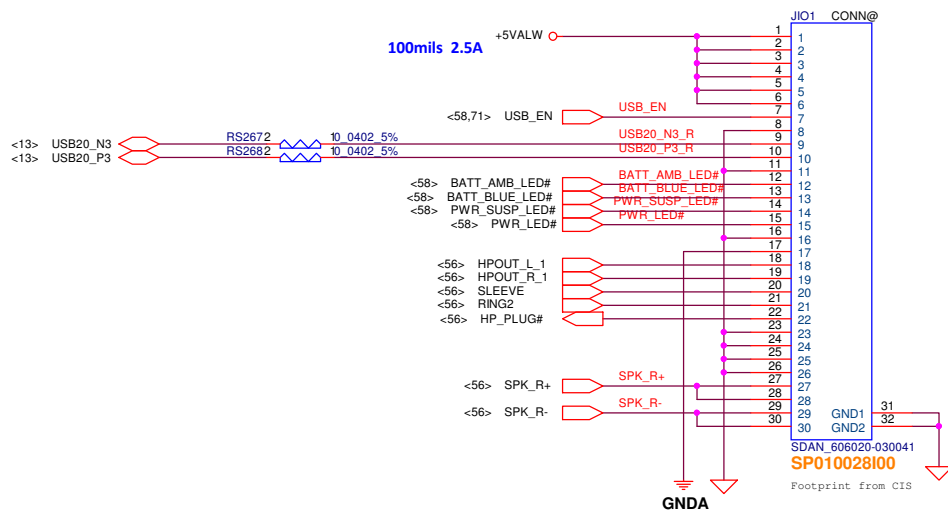
USB3.0 Conn.



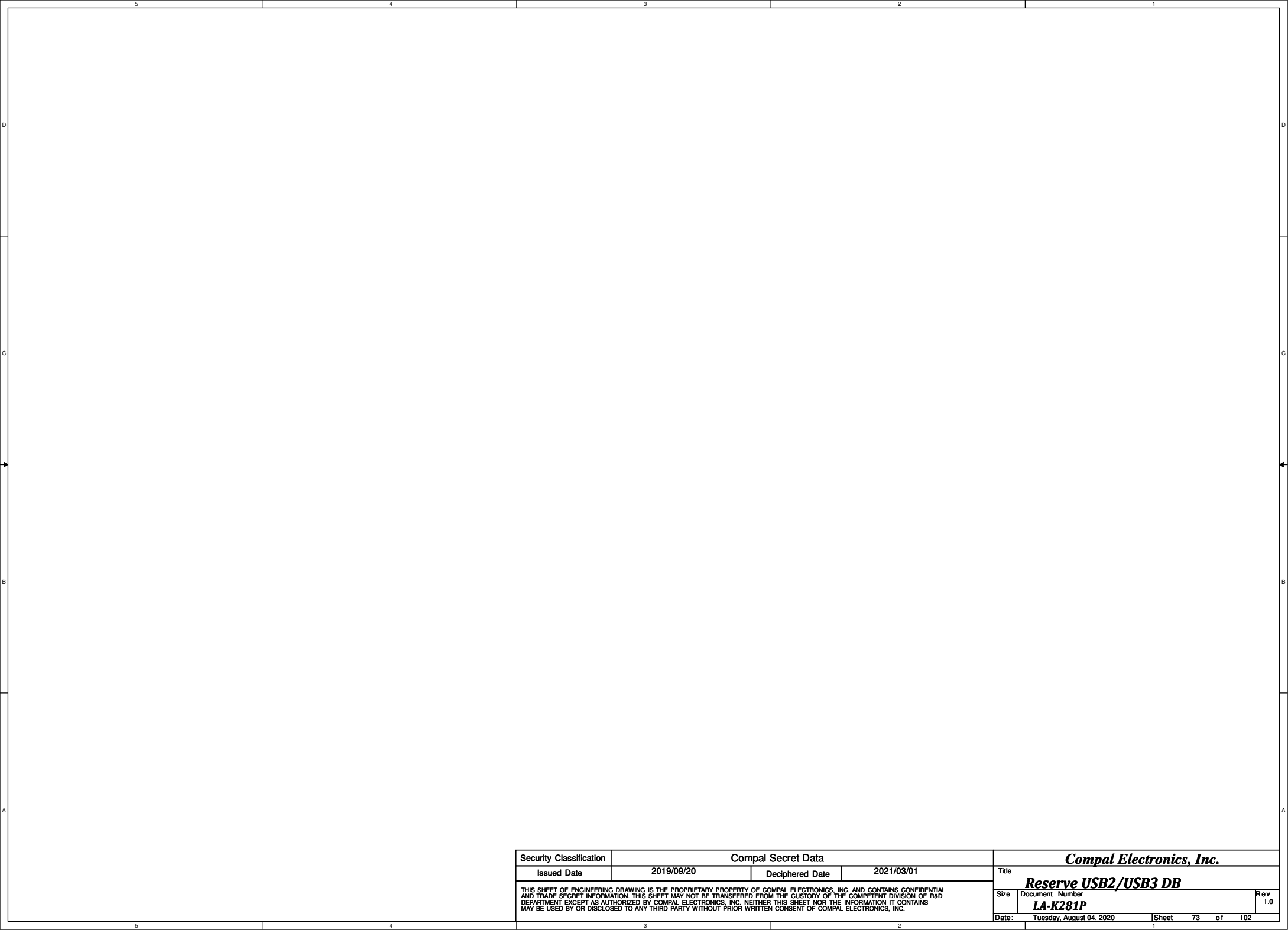
USB Host Charger Truth Table

CHG_EN	CTL1	CTL2	CTL3	ILIM_SEL	MODE	Current Setting	Limit	Note
0	0	1	0	1	SDP1-OFF	ILIM_H		Port power off
1	0	1	0	1	SDP1	ILIM_H		Data Lines Connected
1	0	1	1	1	DCP Auto	ILIM_H		Data Lines Disconnect
1	1	1	1	1	CDP	ILIM_H		Data Lines Connected

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				Sheet	LA-K281P	
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						Size		Document Number		Rev	
						LA-K281P		1.0			
						Date:		Tuesday, August 04, 2020		Sheet 72 of 102	



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								Size		Document Number		Rev	
								LA-K281P				1.0	
								Date:		Tuesday, August 04, 2020		Sheet 73 of 102	



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								Size		Document Number		Rev	
								LA-K281P				1.0	
								Date:		Tuesday, August 04, 2020		Sheet 74 of 102	



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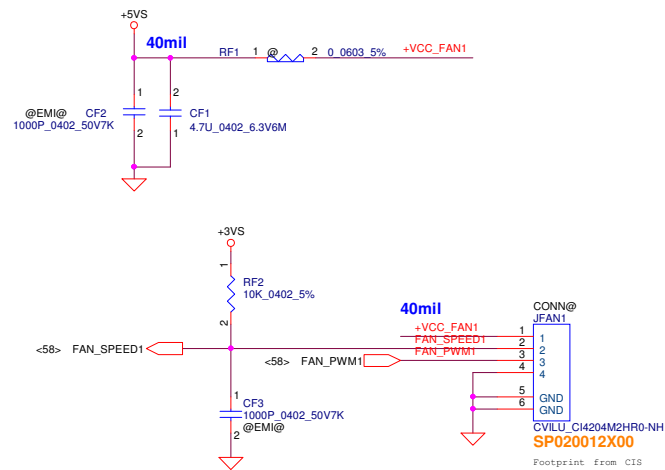
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						Reserve for USB				
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						LA-K281P				
						Rev 1.0				
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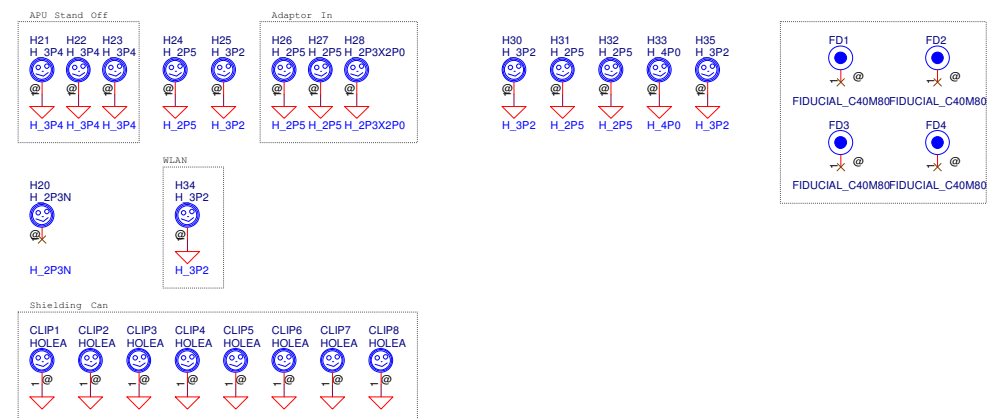


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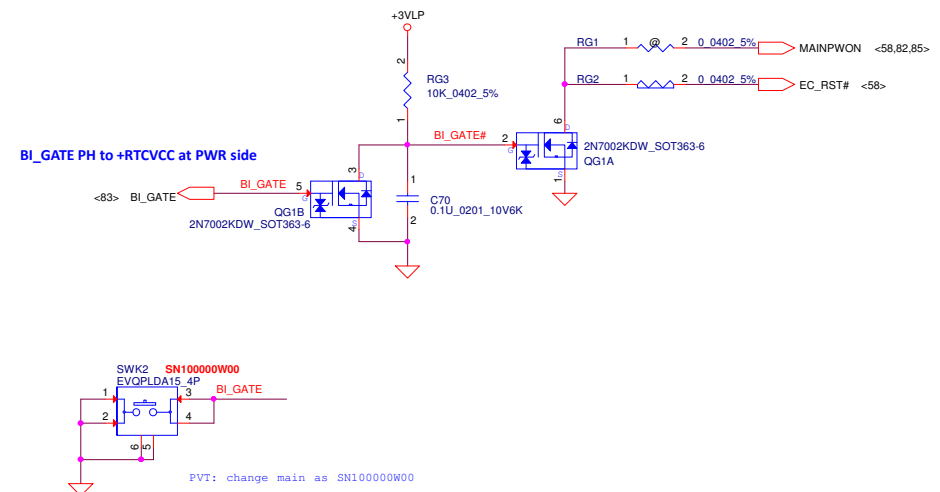
FAN Conn



Screw Hole



Reset Circuit



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+3VALW TO +3VS

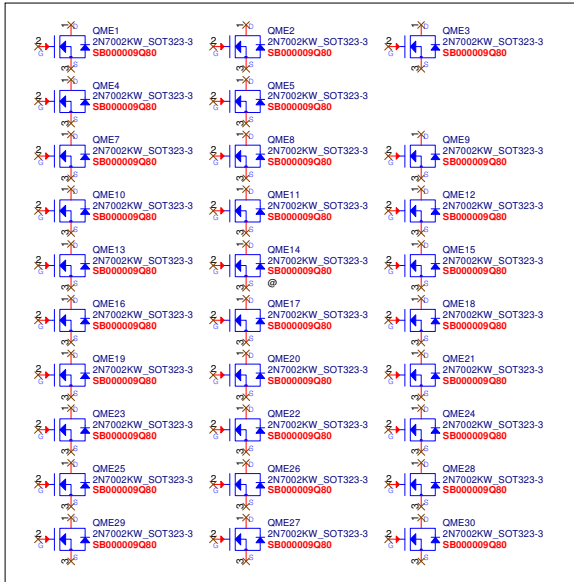
+1.8VALW_PRIM TO +1.8VS

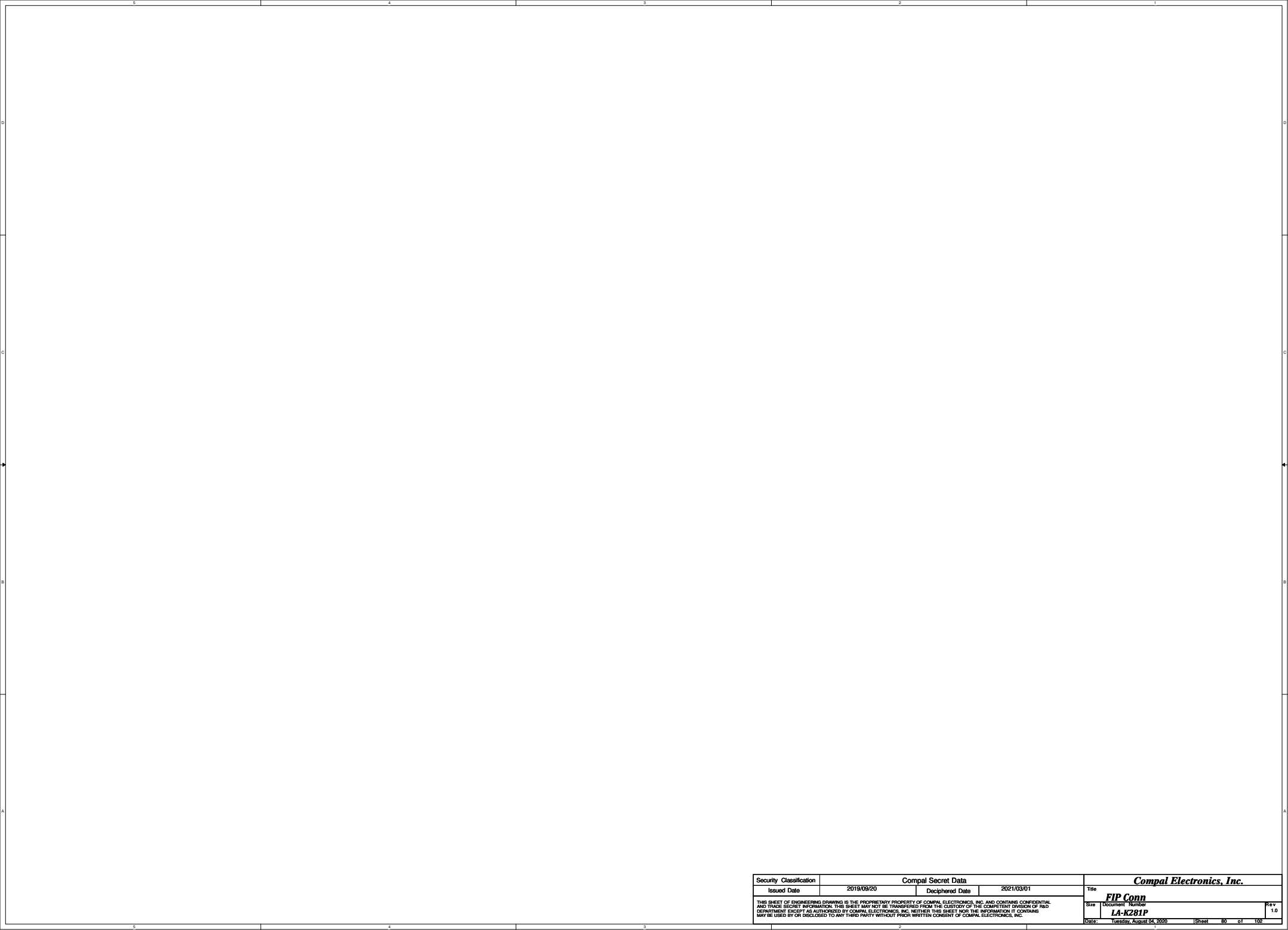
+5VALW TO +5VS

DIS (1.8VSDGPU_AON and +1.8VSDGPU_MAIN), remove

ME Keyboard Braket Support

Place below component at Keyboard support white paint area.

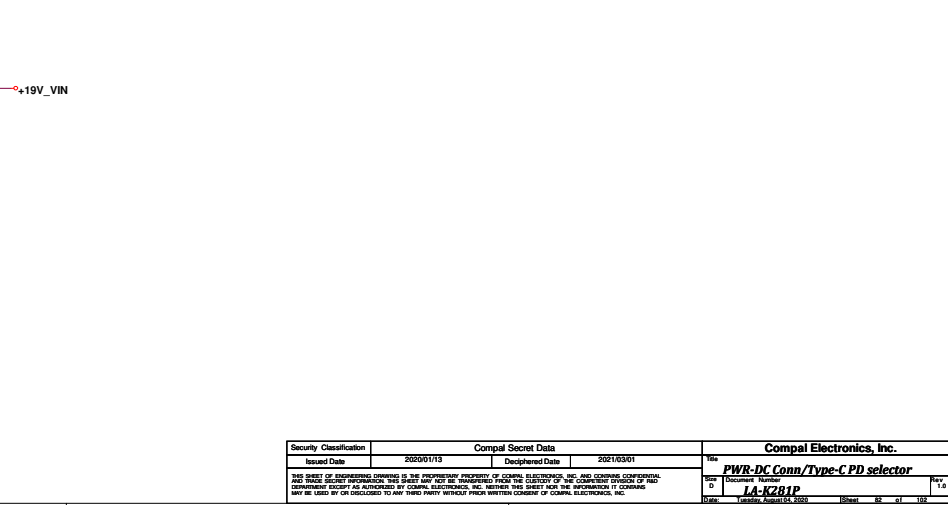
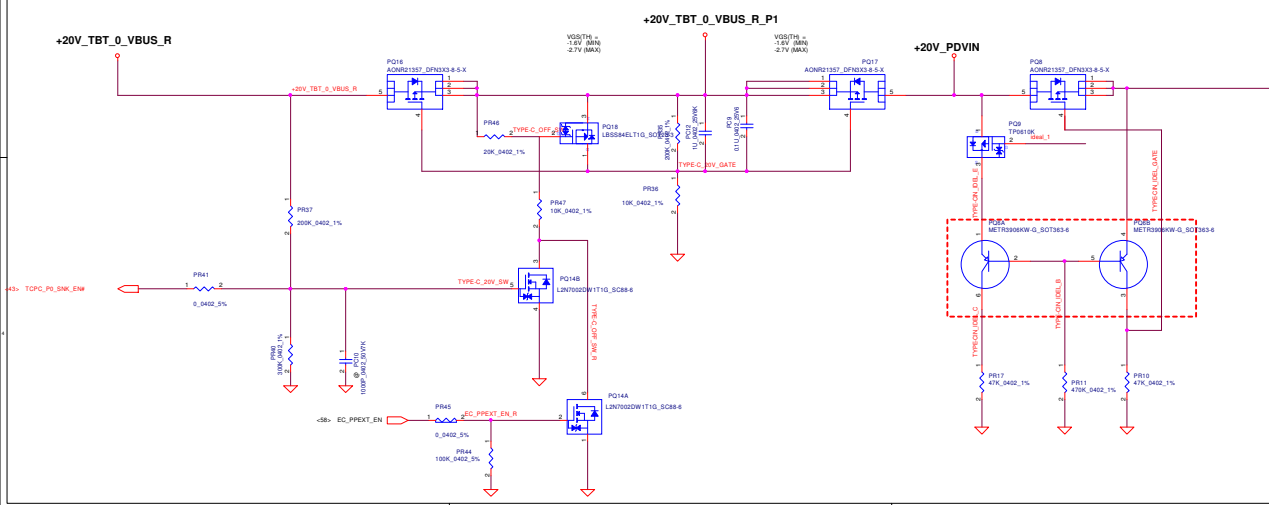
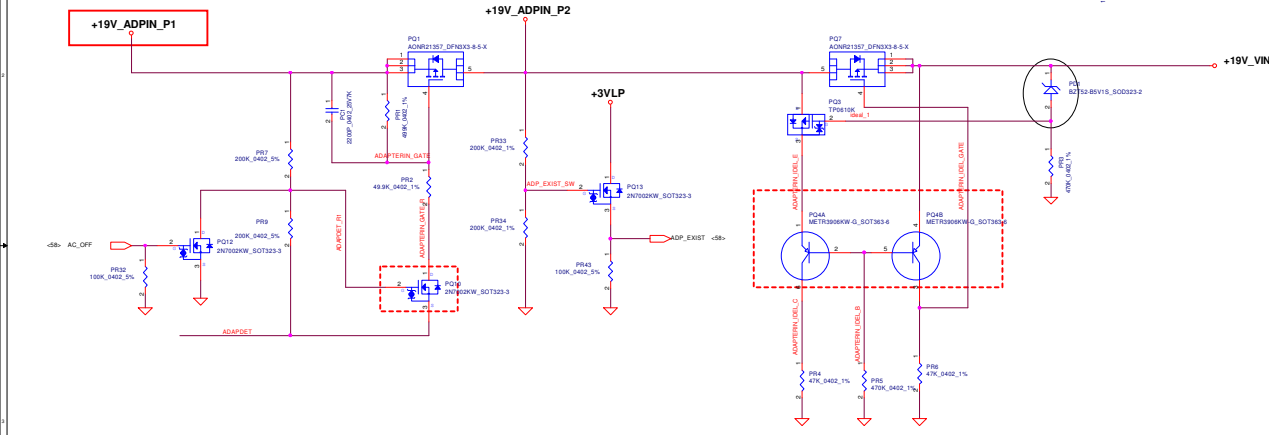
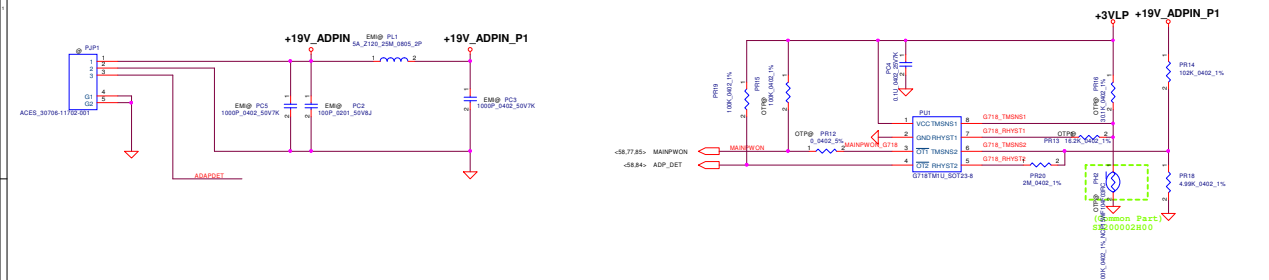




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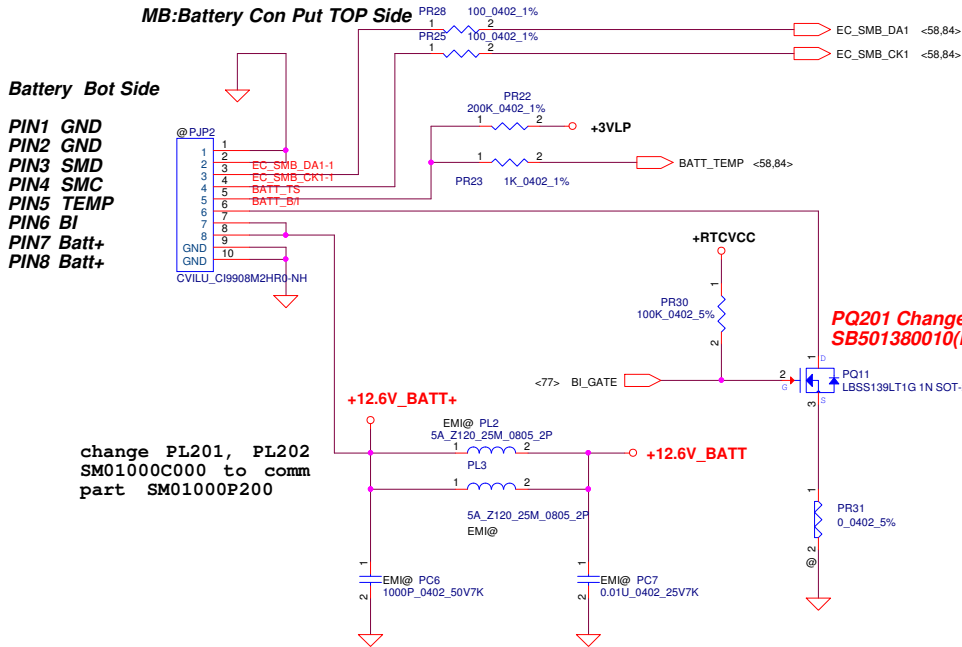
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EC 控制 ○ 功率器件封装

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				LA-K281P	
				Rev	1.0



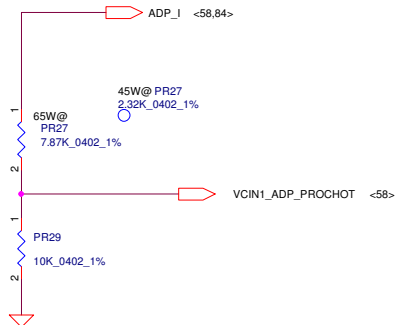
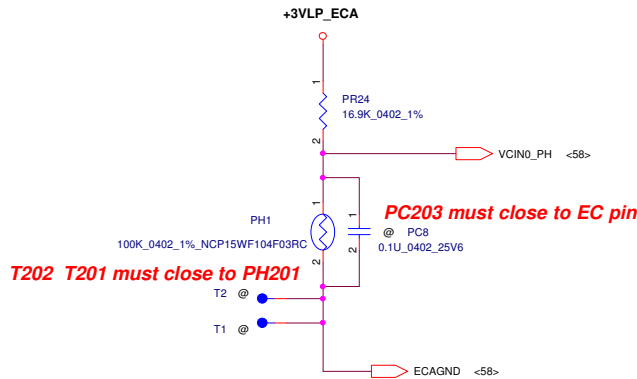
2013/06/07
Add for ENE9022 Battery Voltage drop detection.
Connect to ENE9022 pin64 AD1.

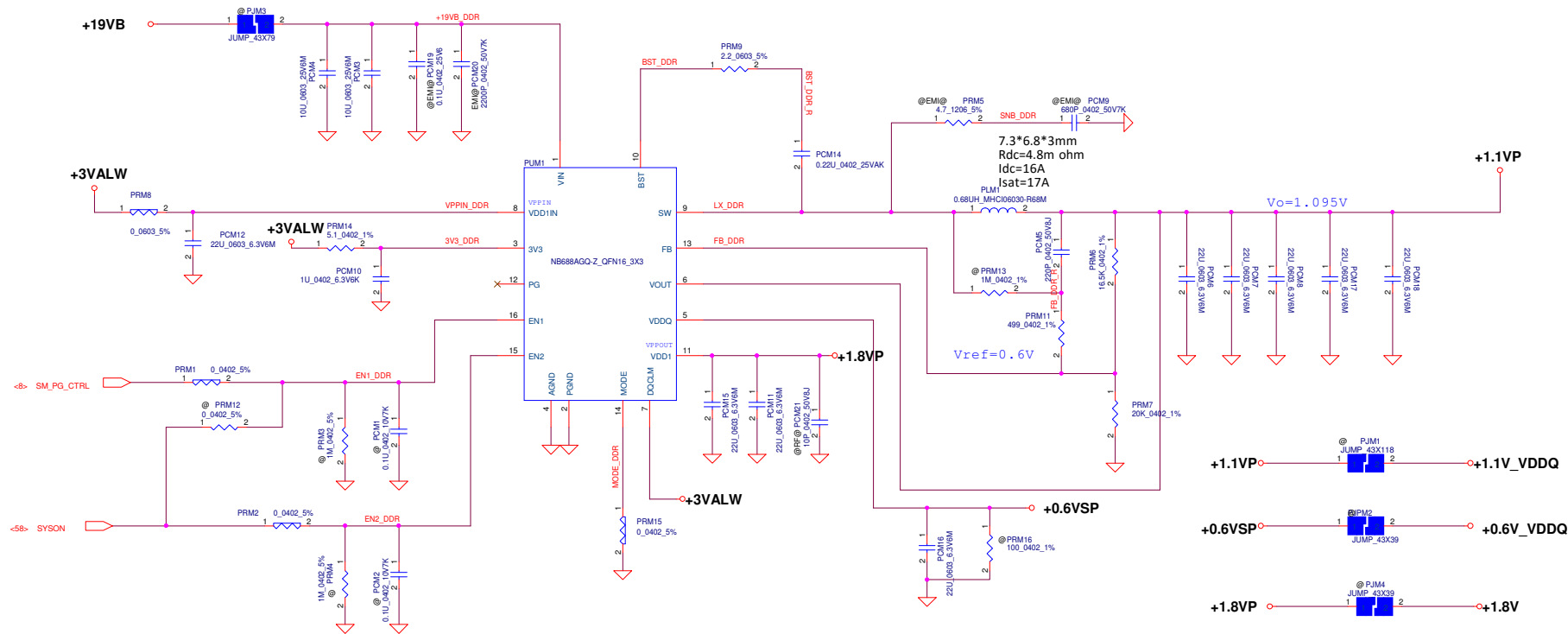


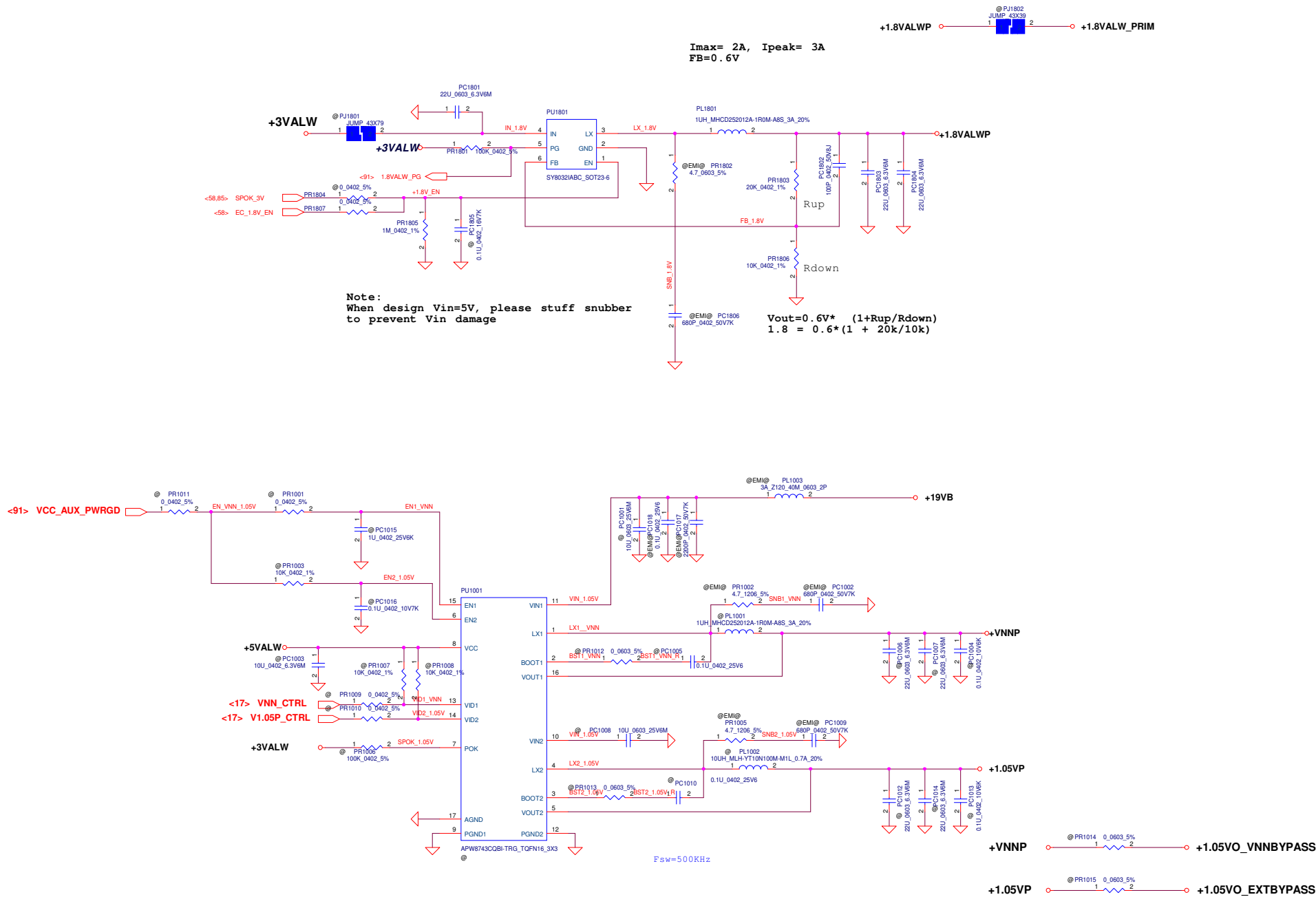
2016/11/16 update

For KB9022 sense 20mΩ	Active	Recovery
45W PR206 2.32K ohm	58.5W, 1V	Active=recovery
65W PR206 7.87K ohm	84.5W, 1V	Active=recovery
90W PR20K ohm	__W, __V	Active=recovery
PH1	2V	1V

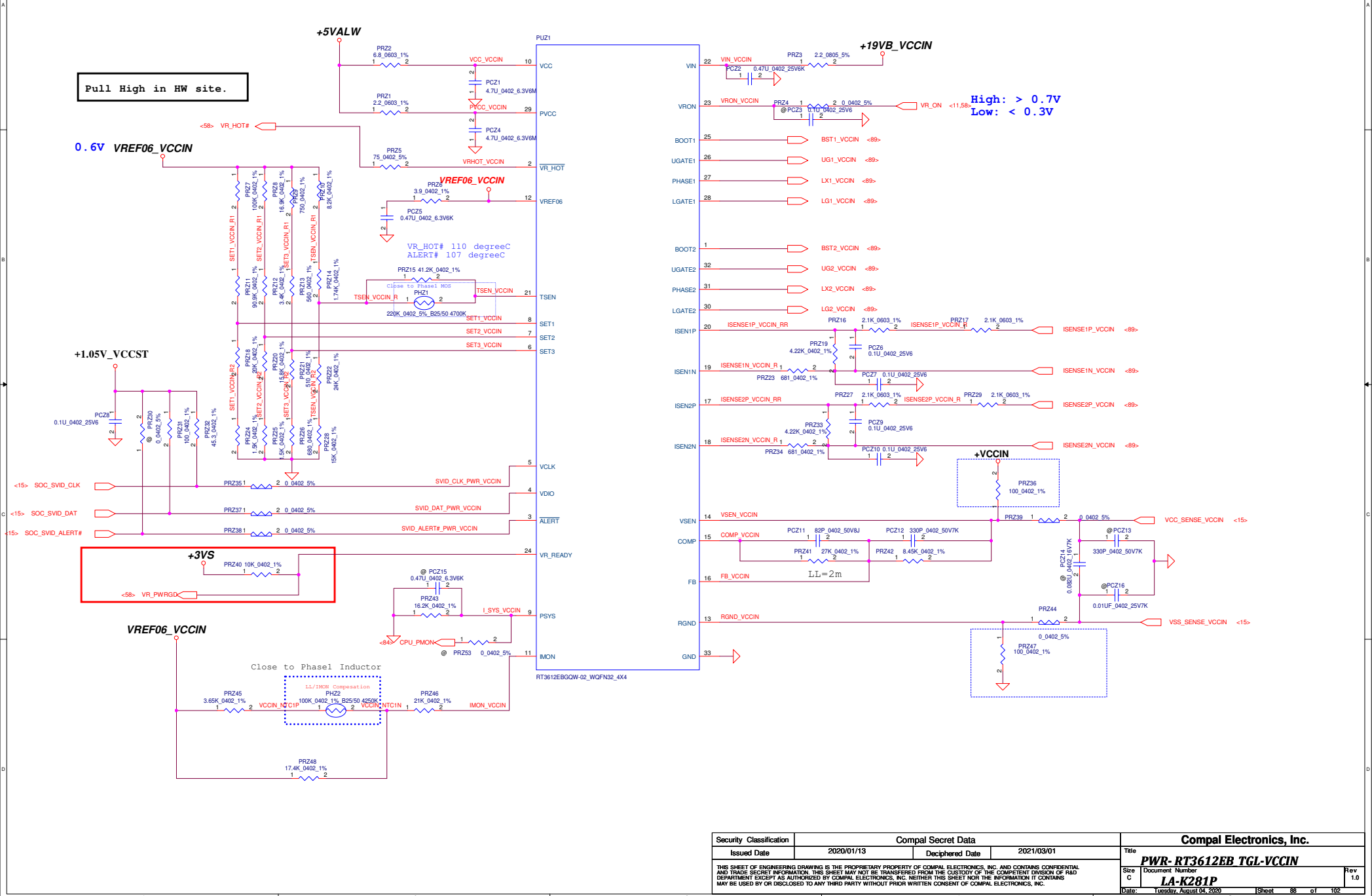
PH1 under CPU bottom side :
CPU thermal protection at 89 +-3 degree C
Recovery at 56 +-3 degree C





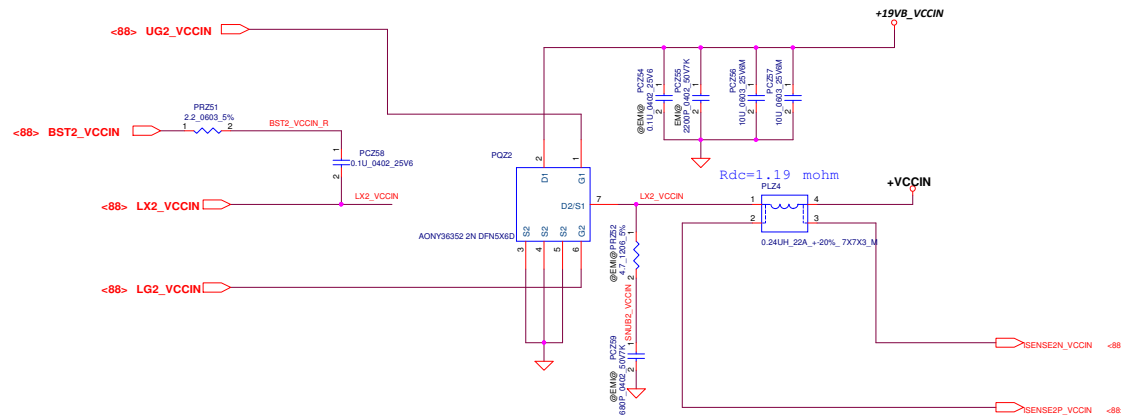
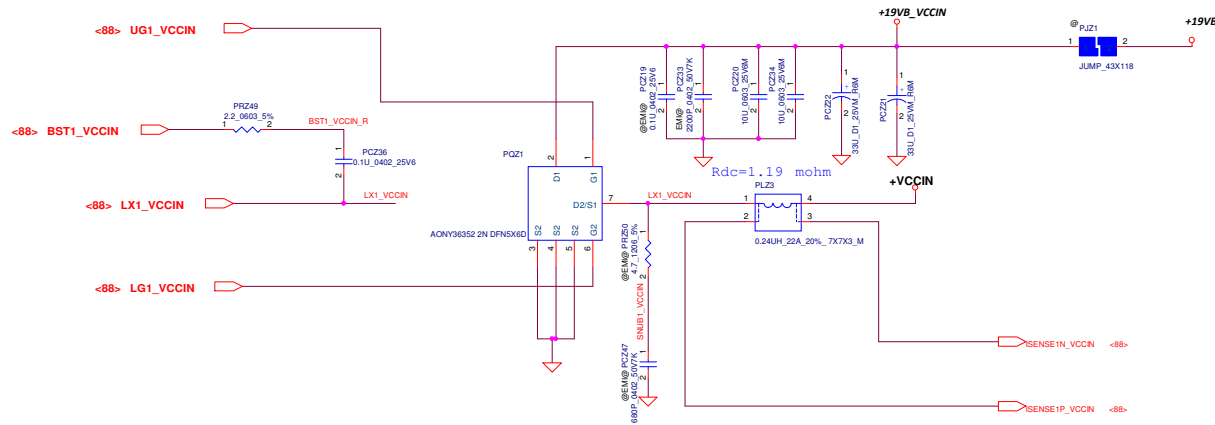
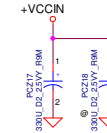


Module model information
RT3612EB_2Phase_V1A.mdd for IC portion
RT3612EB_2Phase_V1B.mdd for SW portion



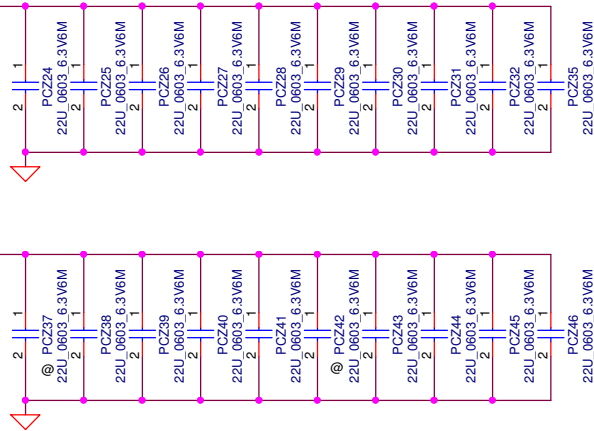
Frequency 600KHz

ICCMAX=54A
TDC=25A
OCP=160% of Iccmax=86.4A
OVP=VID+0.35V=2.24V

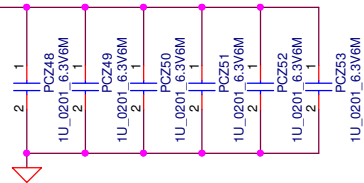


330U_R9 *1
22U_0603 *18
1U_0201 *6

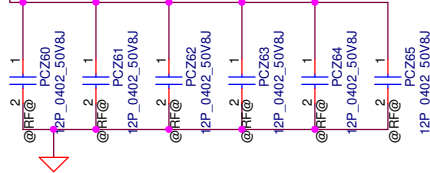
+VCCIN



+VCCIN



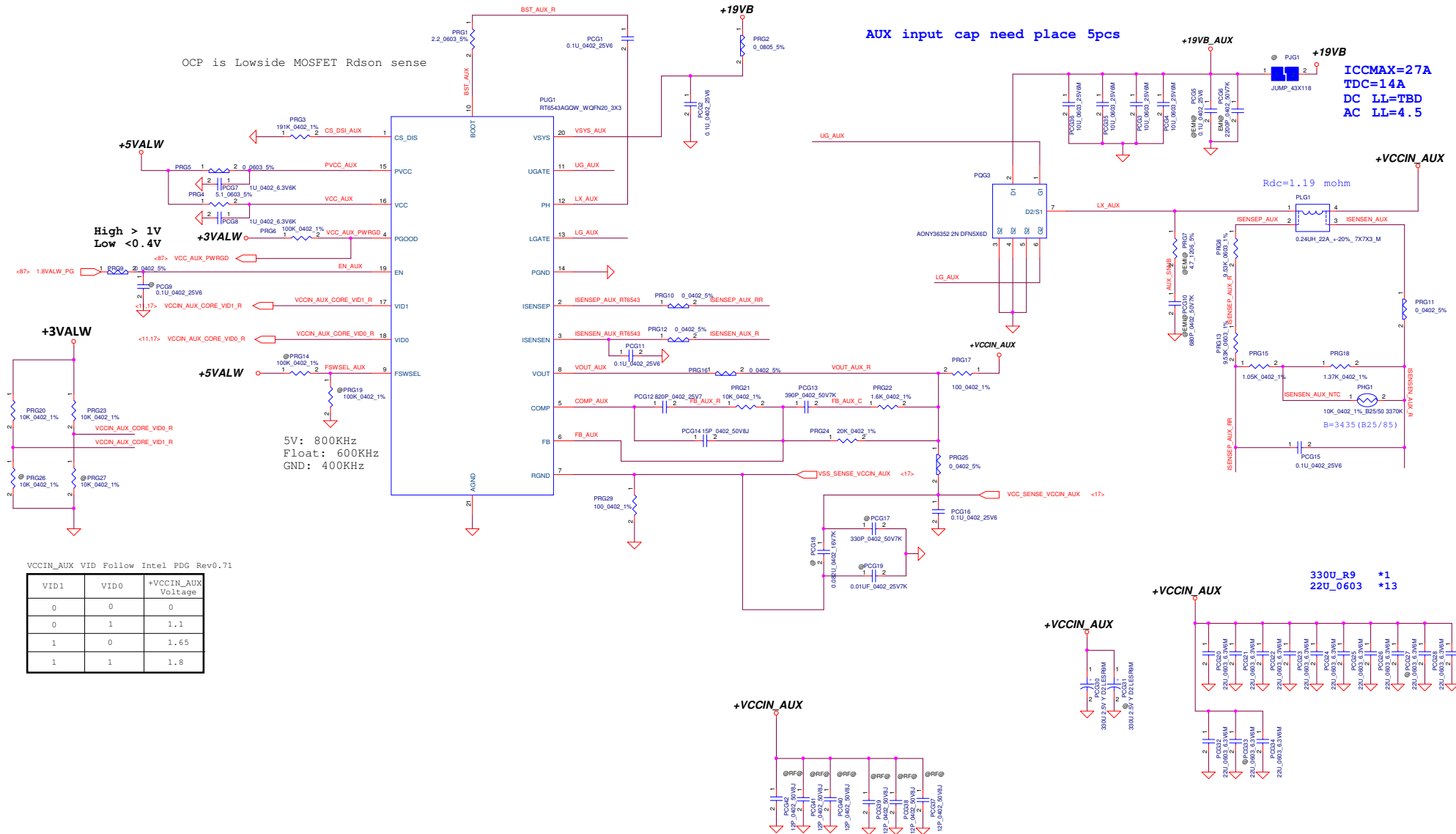
+VCCIN



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Module model information
RT6543A_V1A.mdd for IC portion
RT6543A_V1B.mdd for SW portion
```

OCP is Lowside MOSFET Rdson sense

VCCIN_AUX VID Follow Intel PDG Rev0.71

VID1	VID0	+VCCIN_AUX Voltage
0	0	0
0	1	1.1
1	0	1.65
1	1	1.8

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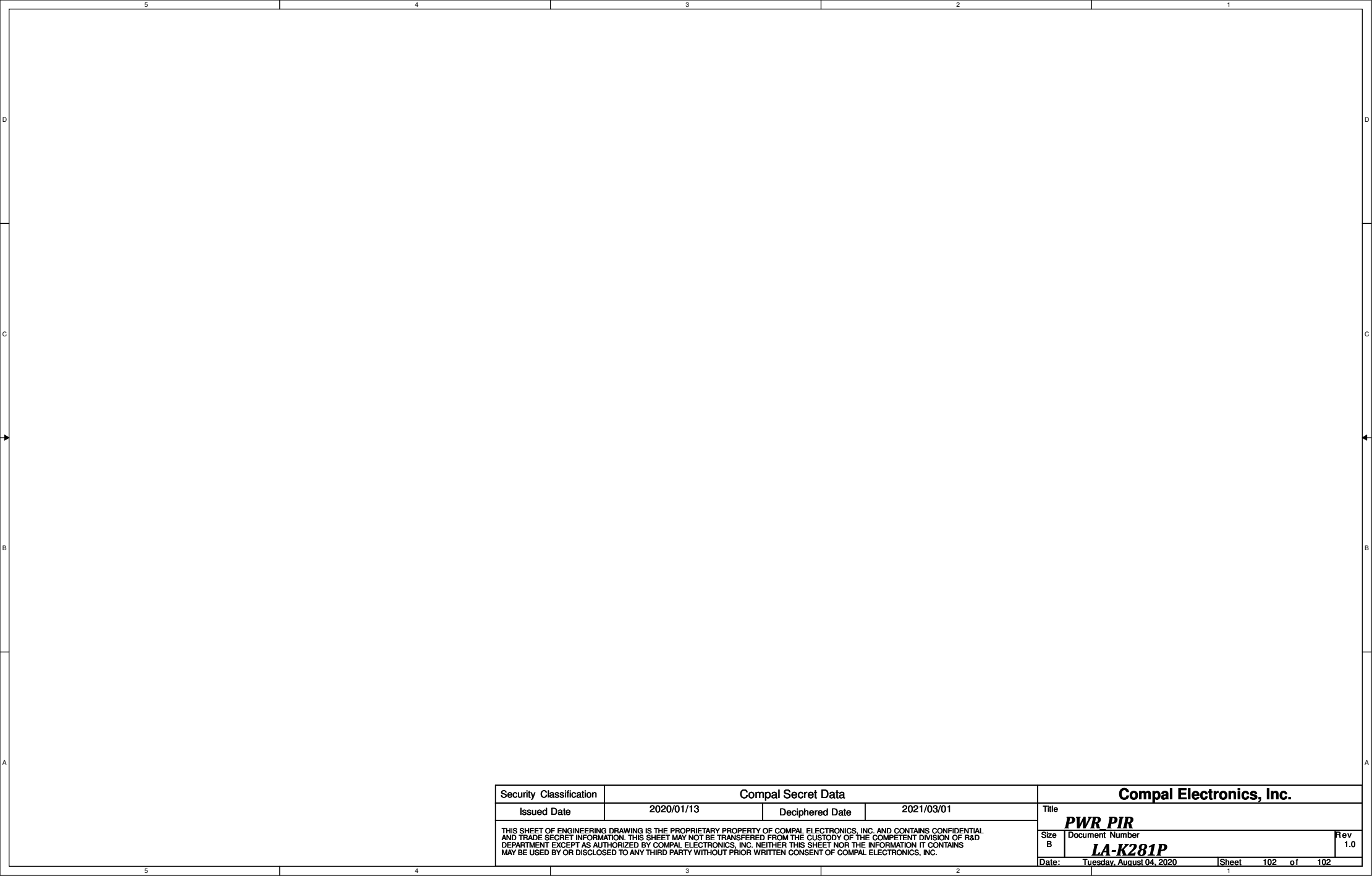
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Version change list (P.I.R. List)

Item	Fixed Issue	Reason for change	Rev.	PG#	Modify List	Date	Phase
01		Battery cell pin setting		P084	PRB20 change to SD00000DM00	20200601	EVT 2
02		CPU_CORE transient test		P088	PRZ46 change to SD034210280 Add PCZ21 (SGA0000A400)	20200601	EVT 2
03		change main source		P082	PQ14 change to SB00000EO00	20200601	EVT 2
04		Sourcer request		P084	PCB29 change to SE00000TB00 PC2 change to SE00000SE00	20200601	EVT 2
05		Design change			PRG2, PRG5, PRM8, PR38,PR41,PR45,PRB13,PRB21,PRB23,PRB25,PRB26,PRB6, PRB7,PRG10,PRG11,PRG12,PRG16,PRG25,PRG9,PRM1,PRM15,PRM2,PRZ35, PRZ37,PRZ38,PRZ39,PRZ4,PRZ44 change to short pad	20200601	EVT 2
06		Design reserve			Reserve PCG33,PCG27 and PCB36	20200601	EVT 2
07							
08							
09							
10							
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